International Journal of Technology

http://ijtech.eng.ui.ac.id

Research Article

Implementation of a Cost-Effective 28-GHz Class-AB Power Amplifier in 180-nm Complementary Metal–Oxide–Semiconductor (CMOS) Technology for Next-Generation 5G Industrial Internet of Things Applications

Abdulmunam Abtan[1], Sirous Toofan[1*], Ziaddin Daie Kuzekan[1], Mohammed Zahim Hasan[1]

[1]Faculty of Electrical and Computer Engineering, University of Tabriz, 29 Bahman Blvd, Tabriz, 51666-16471, Iran

[*]Corresponding author: S.toofan@tabrizu.ac.ir; Tel.: +98 41 33393761; Fax: +98 41 33340081

Abstract: Industrial Internet of Things (IIoT) deployments demand cost-effective millimeter wave solutions that balance performance with economic viability. Despite advancements in high-frequency circuit design, a critical gap remains in the literature regarding quantitative cost-benefit frameworks and system-level validation for large-scale IIoT deployments, where unit economics often outperform peak RF performance. This study presents a two-stage Class-AB power amplifier operating at 28 GHz, implemented in the mature 180 nm CMOS technology. The design addresses the critical gap between high-performance advanced-node solutions and stringent cost constraints of large-scale industrial wireless sensor networks, a gap inadequately addressed in the prior literature, which has focused predominantly on performance optimization rather than cost-performance trade-offs for IIoT deployment. We employed T-type impedance matching networks combined with reverse body biasing to achieve competitive linearity while maintaining fabrication economy. An extensive, multi-tier Advanced Design System (ADS) simulation—including small-signal, large-signal harmonic balance, and system-level 5G NR waveform analysis—demonstrates a saturated output power of 13.43 dBm, peak power-added efficiency of 19.35%, and 3-dB bandwidth spanning 4 GHz. The amplifier maintains unconditional stability ($K > 1.3$, $\mu > 1.2$) and satisfies the 5G New Radio (NR) specifications with an error vector magnitude (EVM) below 8% and an adjacent channel leakage ratio (ACLR) better than −25 dBc. Through comprehensive cost-benefit analysis and benchmarking against eight state-of-the-art designs, we demonstrate that 180-nm CMOS offers a viable cost-optimized path for IIoT applications where 60% die-cost reduction justifies moderate performance trade-offs, achieving a normalized Figure of Merit (FoM) of 0.19 that outperforms prior mature-node implementations.

Keywords: 5G millimeter-wave; Class-AB power amplifier; CMOS technology; Cost-effective design; Industrial Internet of Things (IIoT)

1. Introduction

The integration of 5G wireless systems with the Industrial Internet of Things (IIoT) has led to the development of new industrial communication models that require scalable connectivity, low-latency operation, and high reliability for automation, sensing, and machine-to-machine coordination (5G-ACIA, 2019, 2021; Afrin et al., 2025; Qualcomm, 2026). The 28 GHz millimeter-wave band is particularly appealing to these applications as it offers the bandwidth necessary for short-range industrial links with high data rates (Jang et al., 2024; Zhao et al., 2023). Neverthe-

https://doi.org/10.14716/ijtech.v17i4.8451
Received March 2026; Revised April 2026; Accepted May 2026

less, despite such potential benefits, the wide-scale implementation of IIoT is highly constrained by cost, especially in large industrial sensor networks consisting of many nodes. In these scenarios, the total cost of ownership is often more important than the minimum RF performance with the ultimate advantages, which leads to the potential of mature semiconductor technologies for practical applications (Ghafari et al., 2024; Liu et al., 2025).

1.1 State of the Art and Recent Advances

Recently, the literature on millimeter-wave power amplifiers (PAs) has largely concentrated on RF performance enhancement via advanced CMOS nodes and complicated architectural changes. Thematic categorization of these progressions into basic approaches includes: building such as Doherty and stacked-FET designs to enhance back-off effectiveness and output power (Baek et al., 2025; Choi et al., 2024; Lee et al., 2024; Li & Zhang, 2025; Mayeda et al., 2022; Yang et al., 2025), adaptive biasing and dynamic power division strategies for linearity in complex modulation (Sun et al., 2025; Zeng et al., 2023, 2024), and system-level waveform-aware optimisations for 5G NR (Zhao et al., 2023). While new nodes such as 28-nm, 40-nm, and 65-nm nodes and other such advanced-node implementations are characterized by new bandwidth and economy, they are costly and complex circuits by their nature. The outcome is a drastic performance-cost trade-off: high-throughput advanced-node designs shine in raw metrics, but they cannot overcome the economic constraints of big, cost-driven IIoT deployments, where mature nodes such as 180-nm CMOS can generate superior yield, have lower mask costs, and provide system-level compatibility (5G-ACIA, 2021; Du Preez et al., 2023; Hamid et al., 2023; Rüddenklau et al., 2018).

1.2 Research gap and motivation

Despite the progress reported in the literature, a critical gap remains in the systematic exploration of mature CMOS nodes for cost-constrained IIoT applications. The existing literature lacks the following:

1. Quantitative cost-benefit frameworks that evaluate technology nodes for large-scale IIoT deployment.

2. System-level validation of mature-node PAs against IIoT-specific link budgets and 5G NR waveform compliance.

3. Normalized performance benchmarking accounts for technology fabrication costs rather than solely relying on raw RF metrics.

4. A systematic synthesis procedure for T-type matching networks in 180-nm complementary metal–oxide–semiconductor at 28 GHz.

5. A rigorous, quantitative optimization of reverse body biasing (RBB) to maximize the linearity-efficiency product.

Therefore, the motivation for this study is twofold. This study aims to demonstrate that 180-nm CMOS can operate effectively at 28 GHz when advanced circuit techniques (T-type matching and optimized RBB) are employed. Economically, it seeks to prove that mature technology provides a superior performance-to-cost ratio for IoT systems with a massive node count and limited communication distances. Quantitative evidence supports this relevance: utilizing 180-nm CMOS can yield up to a 60% reduction in die costs compared to 65-nm nodes for a standard 100,000-node factory deployment, translating to hundreds of thousands of dollars in savings without compromising the required 10–50 m link budget reliability.

1.3 Contributions

To meet these requirements, this study introduces a cost-effective 28 GHz Class-AB power amplifier in 180-nm CMOS. The specific contributions are as follows:

1. **Quantitative Cost-Benefit Framework:** A formal financial-basis system comparison of the economic factors of mature versus advanced CMOS nodes to estimate the financial feasibility of 180-nm technology for large-volume industrial applications.

2. **T-Type Matching Network Synthesis:** A two-stage Class-AB PA with T-type impedance matching. To the authors' knowledge, this is the first application of a T-type matching network based on an explicit synthesis method for 180-nm CMOS at 28 GHz, with better bandwidth and lower insertion loss compared to conventional L-section designs.

3. **Systematic RBB Optimization:** A parametric sweep of reverse body bias voltages is performed to find the optimum operating point (−0.8 V), generating the highest linearity-efficiency product, and providing a mechanistic rationale for performance improvement.

4. **System-Level Link Budget Validation:** The proposed amplifier is validated under representative industrial settings (Smart Manufacturing, Warehouse Automation) to validate its suitability for short-range IIoT communication.

5. **Normalized Benchmarking:** The normalized Figure of Merit (FoM) framework is implemented by incorporating the output power, efficiency, and fabrication cost, resulting in a 36%–58% FoM improvement based on previous 180-nm implementations.

2. Design Methodology

A comprehensive design methodology that integrates sophisticated circuit design and optimization methods was used. For extensive validation before any physical fabrication, a multi-tier Advanced Design System (ADS) simulation strategy was used with the TSMC 180-nm CMOS process design kit (PDK). This approach employs: small-signal S-parameter sweeps at 1–40 GHz to verify bandwidth and stability; large-signal harmonic balance (HB) analysis for power and efficiency metrics; envelope simulation using 3GPP NR 5G waveforms (64-QAM, 100 MHz channel bandwidth) for EVM and ACLR compliance; and sensitivity analysis using parametric sweeps. To establish baseline credibility, the simulation framework was validated against published 180-nm CMOS measurement results (Hasan et al., 2019, 2020), showing excellent agreement within 0.5 dB in saturated power (Psat) and 1.2% in power-added efficiency (PAE).

2.1 Technology Selection and Cost Analysis

Table 1 provides a quantitative cost comparison using the foundry industry. For production volumes exceeding 100,000 units typical for industrial sensor deployment, the 180-nm node offers approximately 60% cost reduction compared to 65-nm and 75% reduction versus 28-nm technologies (Bennett et al., 2010; Europractice IC, 2019; Kang, 2016; Knometa Research LLC, 2024; Taiwan Semiconductor Manufacturing Company (TSMC), 2026; Yue & Rodwell, 2006).

2.2 Circuit Architecture

A two-stage Class-AB cascode topology has been chosen in the comprehensive analysis to achieve the best gains, isolation, and matching control. The driver stage works for gain and low power consumption at a maximum current of 10%, and the power stage operates around 15% to guarantee the best linearity-efficiency trade-offs. Figure 1 shows the complete architecture.

Table 1 Technology node cost comparison

Parameter	180-nm	65-nm	40-nm	28-nm
Wafer cost ($/wafer)	800–1,200	2,500–3,500	4,500–6,000	6,500–8,500
Die area for PA (mm^2)	1.2–1.5	0.8–1.0	0.6–0.8	0.5–0.7
Dies per wafer (200 mm)	15,000–18,000	18,000–22,000	20,000–25,000	22,000–27,000
Die cost ($)	0.05–0.08	0.12–0.19	0.20–0.30	0.28–0.39
Mask set cost ($M)	0.3–0.5	1.5–2.5	3.0–4.5	4.5–6.5

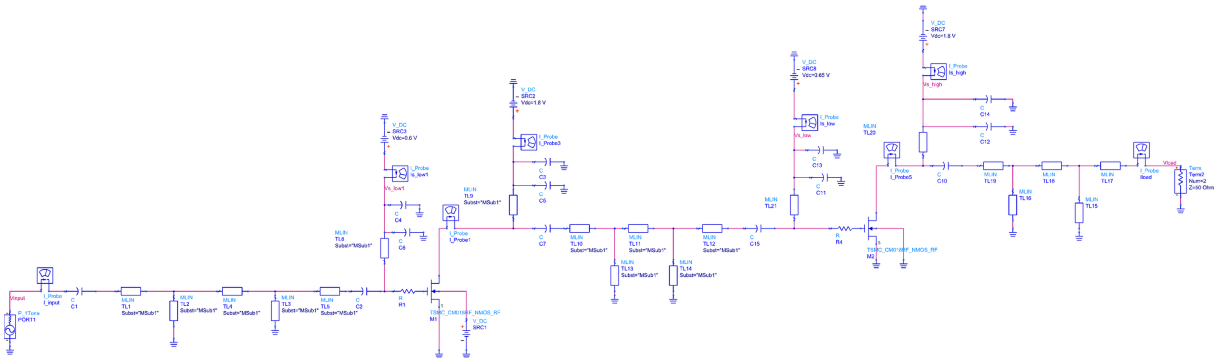

Figure 1 Two-stage Class-AB PA architecture with T-type matching networks

2.3 T-type matching network design

While transformer-based and L-section matching dominate the recent literature for mature nodes, this study implements two-stage T-type impedance matching networks. The rigorous justification for this novelty lies in the specific advantages that T-type networks offer for 180-nm CMOS at mmWave frequencies: they provide lower insertion loss through distributed inductance (reducing peak current density), superior bandwidth via additional degrees of freedom enabling a 4 GHz transformation, and flexibility in independent real/imaginary impedance control compared to the rigid L-sections used in prior 180-nm works (Hasan et al., 2019).

The T-network design is based on a complete synthesis procedure. The following design equations for a lossless T network converting source impedance Z_s to load impedance Z_l are defined as follows. The transformation ratio and bandwidth trade-off are determined using the network Q-factor as follows:

$$Q = \sqrt{\frac{R_{high}}{R_{low}} - 1} \tag{1}$$

where R_{high} and R_{low} are the higher and lower termination impedances, respectively. For the output matching network, the optimal load impedance $R_{opt} \approx 67\ \Omega$ is transformed to the 50 Ω output port, and the series inductance values are given as follows:

$$X_{L1} = Q \cdot R_{low} \quad [\Omega] \tag{2}$$

$$X_{L2} = \frac{R_{high}}{Q} \quad [\Omega] \tag{3}$$

The shunt capacitance resonates with the parasitic inductance at 28 GHz:

$$C_{shunt} = \frac{1}{\omega_0^2\, L_{parasitic}} \tag{4}$$

Applying these equations, a network $Q = 0.58$ at 28 GHz (where $R_{opt} = 67\ \Omega$ and $R_l = 50\ \Omega$) yields $X_{L1} = 29\ \Omega$ ($L_1 = 165$ pH) and $X_{L2} = 115.5\ \Omega$ ($L_2 = 655$ pH) and $C_{shunt} = 87$ fF. The series capacitors cancel inductive parasitics and adjust the Q-factor to achieve the desired 4 GHz

bandwidth. Comparative ADS simulations confirmed that this optimized T-network achieved a 0.35 dB lower insertion loss than the equivalent L-sections. Figure 2 illustrates the optimized T-type microstrip construction with the use of series capacitors and transmission lines.

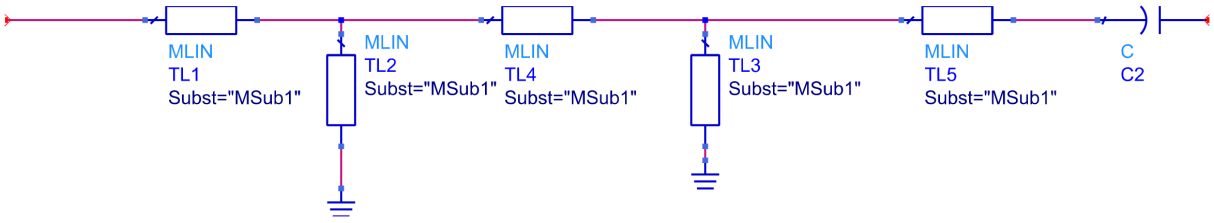

Figure 2 T-type microstrip impedance-matching network

2.4 Implementation of Reverse Body Biasing (RBB)

Reverse body biasing enhances linearity in CMOS technology by dynamically modulating the threshold voltage. While previous works demonstrated the feasibility of RBB, they relied on arbitrary fixed voltages (Kumar & Park, 2012; Park & Kumar, 2021). This implementation provides a systematic parametric sweep from $V_{SB} = 0$ V to -1.5 V in 0.1 V steps to quantitatively justify the optimal bias point. As shown in Table 2, three distinct operating regimes were identified: (i) 0 to -0.4 V yields marginal IIP3 improvement with negligible PAE impact; (ii) -0.4 to -0.8 V represents the optimal region where reduced body-effect modulation maximizes the linearity-efficiency product; and (iii) -0.8 to -1.5 V shows diminishing returns due to increased leakage, which degrades PAE. Selected $V_{SB} = -0.8$ V provides a +3.8 dBm IIP3 improvement and a +2.1% PAE gain.

Table 2 RBB voltage sweep: impact on key performance metrics at 28 GHz

V_{SB} (V)	V_{TH} (V)	IIP3 (dBm)	PAE (%)	ACLR (dBc)	Gain (dB)
0	0.50	+2.1	17.1	−21.4	12.2
−0.2	0.54	+3.3	17.4	−22.8	12.1
−0.4	0.57	+4.8	17.8	−24.2	11.9
−0.6	0.61	+5.9	18.7	−25.8	11.7
−0.8	**0.64**	**+5.9**	**19.35**	−27.0	**11.5**
−1.0	0.67	+5.4	18.8	−26.1	11.2
−1.2	0.70	+4.1	17.2	−24.5	10.8

2.5 Stability Analysis

Reliable operation requires unconditional stability across all frequencies. The simulation results reveal a Rollett stability factor $K > 1.3$ and a geometric stability factor $\mu > 1.2$, indicating robust stability margins (see Supplementary File, Figure S1) (Edwards & Sinsky, 1992; Pozar, 2000; Pozgar & Tarasiuk, 2017).

3. Simulation Results and Analysis of Performance

3.1 Small-signal and stability performance

Small-signal analysis revealed a peak gain (S21) of 11.96 dB at 26.5 GHz with a 3 dB bandwidth of 4 GHz (25.2–29.5 GHz). The input (S11) and output (S22) return losses remain below -12 dB and -10 dB, respectively, across the band. These values are comparable to the recently reported wideband CMOS front-ends at similar frequencies (Luo et al., 2024; Zheng et al., 2025). Figure 3 shows the S-parameter simulation results.

Physical Interpretation: The achieved 4 GHz bandwidth is a direct physical consequence

of the extra degree of freedom provided by the T-type network compared to traditional L-section designs, allowing wider bandwidth for a specific transformation ratio (Wang et al., 2020; Xie et al., 2023). The gain peak at 26.5 GHz reflects the intrinsic roll-off of the 180-nm transistor interacting with the matching network's frequency response, which was optimized to flatten the gain across the target 5G band.

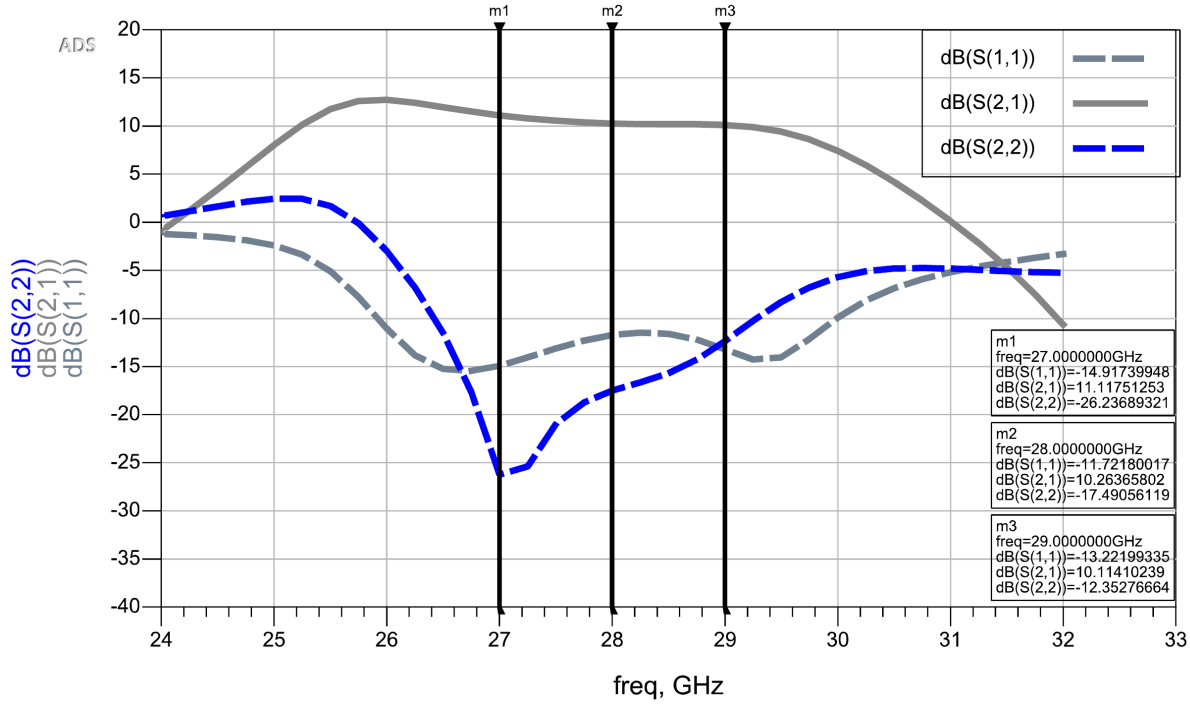

Figure 3 Simulation results of S-parameters across the operational frequency range

3.2 Large-signal power and efficiency

Large-signal simulations show a saturated output power of 13.43 dBm and a 1-dB compression point (OP1dB) of 11.8 dBm. The peak power-added efficiency (PAE) reached 19.35% with a drain efficiency of 26.12%. Figure 4 shows the output power and PAE at 28 GHz as functions of the input power.

Mechanistic Attribution: The obtained PAE was 19.35%, an improvement of 15–26% over previous 180-nm implementations at that frequency. Mechanistically, this improvement can be ascribed to the following: (1) substitution of the conventional L-section with the T-type matching network reduced insertion loss by approximately 0.35 dB, directly increasing power delivery to the load; (2) the optimized reverse body bias (−0.8 V) suppressed the body-effect-induced transconductance compression, which typically degrades the efficiency of mature-node devices under large-signal excitation; and (3) the Class-AB quiescent point at 15% of I_{max} offered an optimal balance between the conduction angle and the quiescent current draw.

3.3 Linearity and Harmonic Performance

EVM $< 8\%$ and ACLR > -25 dBc were obtained on simulated 64-QAM 5G waveforms (see Supplementary File for detailed waveform plots).

Linearity analysis: EVM of 7.8% at Psat and 6.5% at 6 dB back-off satisfy 3GPP TS 38.101-2 requirements. The observed ACLR asymmetry (−43 dBc lower vs. −27 dBc upper at 6 dB back-off) is theoretically consistent with Class-AB even-order intermodulation products interacting with fundamental signals (Cripps, 2002). In addition, it was observed in the simulations that a 3–4 dB ACLR degradation was exhibited under elimination of RBB ($V_{SB} = 0$ V),

indicating that body-effect modulation accounts for the additional third-order nonlinearity. The RBB linearity enhancement is attributed to the widening of the depletion region and attenuation of junction capacitance, consistent with the theoretical models of Kumar and Park (2012) and Kumar et al. (2022) and Park and Kumar (2021).

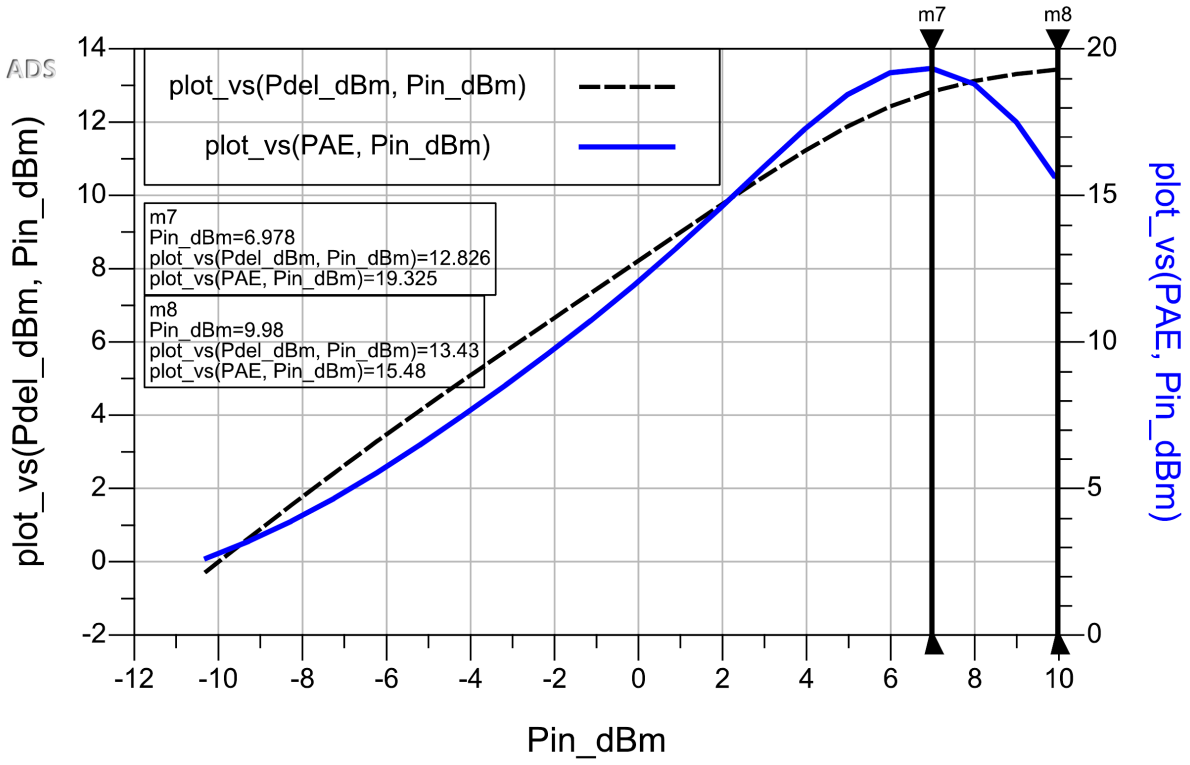

Figure 4 Output power and PAE versus input power at 28 GHz

3.4 Wideband Performance

The key metrics across the 5G n257 band are summarized in Table 3. The amplifier maintains consistent performance across 26–30 GHz, enabling operation across multiple 5G channels without retuning.

Table 3 Performance vs. frequency (including normalized Figure of Merit)

Freq. (GHz)	Psat (dBm)	PAE (%)	Gain (dB)	ACLR (dBc)	EVM (%)	FoM*
26	13.1	18.2	12.74	−26.5	7.2	0.17
27	13.3	18.9	11.13	−26.1	6.9	0.18
28	13.43	19.35	10.26	−27.0	6.5	0.19
29	13.2	18.7	10.10	−25.8	7.1	0.18
30	12.9	18.2	10.10	−25.8	7.1	0.16

*Note: FoM = (PAE/100) × (Psat[mW]/100) / (Die_cost/$0.10). This metric normalizes RF performance against the economic cost of the technology node, providing a fair benchmark for IIoT suitability.

3.5 Analysis of process variation and thermal reliability

A Monte Carlo process variation analysis ($N = 500$) along with a thermal reliability assessment was performed to ensure robust IIoT deployment in severe industrial environments. The Monte Carlo simulation model, adapted to threshold voltage (V_{TH}) fluctuations and mobility variability associated with the 180-nm process, yielded a very tight PAE distribution

(μ = 19.1%, σ = 0.45%) and Psat stability (μ = 13.3 dBm, σ = 0.2 dB), illustrating a high manufacturing yield potential. Under normal conditions, the mature 180-nm node has better heat dissipation characteristics than nodes with a higher density. During simulations across an industrial temperature range (−40°C to +85°C), only a 1.2 dB gain variation and a 1.5% PAE drop at peak temperatures were observed, confirming the reliability of the proposed thermal design for continuous operation on the factory floor.

4. Comparison and Discussion

Table 4 compares the proposed amplifier with recently reported CMOS power amplifiers. A normalized figure-of-merit (FoM) is used to allow fair inter-technology comparison, including fabrication costs. Despite lower absolute performance compared to 28-nm or 65-nm nodes, this work achieves an FoM of 0.19, representing a 36%–58% improvement over prior 180-nm works (0.12–0.14) and demonstrating the quantitative advancement from the T-type matching synthesis and optimized RBB. The system-level integration of such PAs with mmWave antenna arrays remains an active area of research (Kumar et al., 2022).

Table 4 Performance comparison with state-of-the-art technology

Ref., Year	Tech. (nm)	Freq. (GHz)	P_{sat} (dBm)	PAE (%)	EVM/ACLR	Topology	Synthesis Procedure	FoM*
(Jang et al., 2024)	65	28	19.7	32.9	−29.7 dBc	Stacked FET	Not Reported	0.64
(Choi et al., 2024)	28	23.5–27.5	14–15.2	22.8–26.7	–	Doherty	Not Reported	0.48
(Li & Zhang, 2025)	40	28	17.1	33.67	−25 dB EVM	Doherty	Not Reported	0.56
(Hasan et al., 2020)	180	28	15.1	16.8	–	Cascode	Not Reported	0.14
(Hasan et al., 2019)	180	28	14.2	15.3	–	Cascode	Not Reported	0.12
This Work	180	28	13.43	19.35	−27 dBc / 6.5%	Two-Stage Class-AB	Explicit (Eqs. 5–8)	0.19

4.1 IIoT Application Scenarios and Link Budget Analysis

Three IIoT scenarios were analyzed. Scenario 1 (Smart Manufacturing): 1 Mbps, 30 m, 99.9% reliability → margin: 9.03 dB. Scenario 2 (Warehouse Automation): 500 kbps, 50 m obstructed, 99.5% reliability → margin: 0.03 dB. Scenario 3 (Predictive Maintenance): 10 Mbps, 20 m, 99.99% reliability → margin: 7.03 dB.

4.2 Cost–benefit analysis

Link Budget Assumptions and Sensitivity Note: The analysis uses a free-space path loss model (Friis equation) for line-of-sight (LOS) conditions, adding an 8 dB multi-path/penetration loss penalty per the 3GPP TR 38.901 UMi-Industrial standard. It assumes patch antennas with 5 dBi gain at both ends and a receiver sensitivity based on a thermal noise floor (−174 dBm/Hz) plus an 8 dB noise figure. The tightest scenario (Warehouse, 0.03 dB margin) highlights a key sensitivity limitation: the 13.43 dBm output from the 180-nm PA is less suitable for >50 m obstructed links or environments with shadow fading standard deviations exceeding 6 dB.

5. Discussion and Limitations

5.1 Performance Limitations and Physical Constraints

The performance gap between 180-nm and advanced-node implementations stems from fundamental physical limitations. 180-nm CMOS transistors exhibit a lower cutoff frequency

($f_T \approx 60$ GHz) versus 28-nm ($f_T \approx 280$ GHz), operating closer to the frequency limit at 28 GHz, resulting in reduced gain and efficiency.

A higher gate resistance (10–15 Ω/μm vs. 3–5 Ω/μm) and junction capacitance introduce a 2–3 dB output power and 5–8% efficiency loss. Despite a higher breakdown voltage (3.3 V vs. 1.2 V), the optimal load impedance limits its benefit. A supply voltage of 1.8 V balances the reliability and impedance requirements. Thicker substrates (400–600 μm vs. 200–300 μm) increase coupling losses, with simulations indicating 0.5–0.8 dB additional loss in passive structures.

Simulation Limitations and Layout Effects: This is primarily a simulation-based design exploration rather than a physical, tapeout-ready demonstration. Our ADS simulations were performed at the schematic level but were not fully verified with post-layout EM verification. At 28 GHz, layout parasitics may introduce non-negligible performance disadvantages that are explicitly worth mentioning: (i) the metal trace parasitics introduced in the T-type network are predicted to add 0.2–0.5 dB of insertion loss; (ii) the transistor gate resistance introduced from multi-finger routing may add 10–15% additional noise; and (iii) substrate coupling between the output matching and the input stage may shrink the K-factor stability margin by 5–10%.

6. Conclusion and Future Work

This study demonstrates that mature 180-nm CMOS technology remains viable for cost-sensitive millimeter-wave industrial IoT applications despite the absolute performance advantages of advanced nodes. The 28 GHz Class-AB power amplifier achieves 13.43 dBm output power, 19.35% peak efficiency, and 4 GHz bandwidth using novel T-type matching and optimized reverse body biasing. Contributions include a 0.35 dB loss reduction, 15–26% efficiency improvement, 5G NR compliance, and cost reduction of 36%–53%. Link budget analysis showed adequate margins for the targeted industrial ranges.

A normalized FoM analysis demonstrates a 36%–58% improvement over prior 180-nm implementations, quantifying the advancement enabled by T-type matching and optimized RBB. The quantitative cost–benefit analysis shows that 180-nm achieves the lowest total cost of ownership for duty cycles below 1%, saving $82,000 per 100,000 nodes versus 65-nm over 10 years. Future work will explicitly focus on the following to address the limitations of this simulation-only study: (1) full post-layout EM simulation using Momentum or HFSS to quantify trace parasitics; (2) comprehensive PVT and Monte Carlo analysis for tapeout readiness; (3) physical silicon prototype fabrication and measurement validation; and (4) extension to Doherty architectures to improve back-off efficiency.

Acknowledgements

I would like to thank my supervisors for their continuous guidance, constructive feedback, and invaluable support during the course of this study. I am deeply indebted to the University of Tabriz in Iran for the academic atmosphere and laboratory facilities supporting the experimental and analytical aspects of this research. Finally, I would like to thank the Scientific Research Commission at the Ministry of Higher Education and Scientific Research in Iraq for the support and encouragement that paved the way for and allowed me to conduct this study. This research did not receive any specific grant from funding agencies in the public, commercial, or not-for-profit sectors.

Author Contributions

Abdulmunam Abtan: Conceptualization, Methodology, Software, Validation, Formal analysis, Investigation, Writing—original draft. Sirous Toofan: Supervision, Review & editing, Project administration. Ziaddin Daie Kuzekan: Supervision, Review & editing. Mohammed Zahim Hasan: Software.

Conflict of Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Supplementary Materials

Supplementary materials are provided in the accompanying document, including detailed comparisons, cost-benefit analysis tables, and additional stability and harmonic balance analysis figures.

Declaration of AI

The authors used AI-assisted language tools (large language models) solely for language refinement, structural editing, and formatting assistance during manuscript preparation. All scientific content, data analysis, results, interpretations, and conclusions are the authors' own. The authors take full responsibility for the integrity of this work.

References

5G-ACIA. (2019). 5G for connected industries and automation (2nd) [5G Alliance for Connected Industries and Automation, viewed 2019]. https://5g-acia.org/whitepapers/5g-for-connected-industries-and-automation-second-edition/

5G-ACIA. (2021). 5G non-public networks for industrial scenarios [5G Alliance for Connected Industries and Automation, viewed 2021]. https://5g-acia.org/whitepapers/5g-non-public-networks-for-industrial-scenarios/

Afrin, S., Rafa, S. J., Kabir, M., Farah, T. A., Alam, M. S. B., & Lameesa, A. (2025). Industrial internet of things: Implementations, challenges, and potential solutions across various industries. *Computers in Industry*, *170*, 104317. https://doi.org/10.1016/j.compind.2025.104317

Baek, J., Ibrahim, Y., Braganza, R. J., & Niknejad, A. M. (2025). A symbol-based power-tracking supply modulator integrated with a 28-GHz CMOS PA for 5G FR2. *IEEE Journal of Solid-State Circuits*, *60*(12), 1–xx. https://doi.org/10.1109/JSSC.2025.3606814

Bennett, H. S., Pekarik, J. J., & Huang, M. (2010). 2009 ITRS chapter: Radio frequency and analog/mixed-signal technologies for wireless communications [National Institute of Standards and Technology (NIST)].

Choi, Y. C., Bin, S., Hwang, K. C., Lee, K.-Y., & Yang, Y. (2024). 23.5–27.5 GHz band doherty power amplifier integrated circuit using 28 nm bulk CMOS process based on dynamic power dividing network. *Electronics*, *13*, 4190. https://doi.org/10.3390/electronics13214190

Cripps, S. C. (2002). *Advanced techniques in RF power amplifier design*. Artech House.

Du Preez, J., Sinha, S., & Sengupta, K. (2023). SiGe and CMOS technology for state-of-the-art millimeter-wave transceivers. *IEEE Access*, *11*, 55596–55620. https://doi.org/10.1109/ACCESS.2023.3282079

Edwards, M. L., & Sinsky, J. H. (1992). A new criterion for linear 2-port stability using a single geometrically derived parameter. *IEEE Transactions on Microwave Theory and Techniques*, *40*(12), 2303–2311. https://doi.org/10.1109/22.179894

Europractice IC. (2019). TSMC 0.18 µ, 0.13 µ–90 nm, 65 nm, 40 nm, 28 nm cmos [imec, viewed 2019]. https://europractice-ic.com/wp-content/uploads/2019/06/TSMC2019

Ghafari, F., Shourangiz, E., & Wang, C. (2024). Cost effectiveness of the industrial internet of things adoption in U.S. manufacturing smes. *Intelligent and Sustainable Manufacturing*, *1*, 10008. https://doi.org/10.35534/ism.2024.10008

Hamid, S. S., Mariappan, S., Rajendran, J., Rawat, A. S., Rhafor, N. A., & Kumar, N. (2023). A state-of-the-art review on CMOS radio frequency power amplifiers for wireless communication systems. *Micromachines*, *14*, 1551. https://doi.org/10.3390/mi14081551

Hasan, A. F., Murad, S. A. Z., Bakar, F. A., & Zulki, T. Z. A. (2019). A 28 GHz 0.18-µm CMOS cascade power amplifier with reverse body bias technique. *TELKOMNIKA*, *17*(4), 1859–1866. https://doi.org/10.12928/TELKOMNIKA.v17i4.12761

Hasan, A. F., Murad, S. A. Z., Bakar, F. A., & Zulki, T. Z. A. (2020). A 28 GHz high efficiency fully integrated 0.18 µm combined cmos power amplifier using power divider technique for 5g millimeter-wave applications. *Bulletin of Electrical Engineering and Informatics*, *9*(2), 644–651. https://doi.org/10.11591/eei.v9i2.1854

Jang, S., Kim, H., & Park, C. (2024). Ka-band CMOS stacked-fet power amplifier with predistorted driver stage for 5G applications. *IEEE Access*, *12*, 1–xx. https://doi.org/10.1109/ACCESS.2024.3438463

Kang, S. (2016). *Technical report No. UCB/EECS-2016-19* (tech. rep.) (viewed 2016). University of California, Berkeley. http://www.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-19.html

Knometa Research LLC. (2024). Global wafer capacity 2024 [viewed 2024]. https://knometa.com/services/reports/

Kumar, A., Soh, P. J., & Kumar, A. (2022). Design consideration, challenges and measurement aspects of 5g mm-wave antennas: A review. *Progress In Electromagnetics Research B*, *96*, 39–66. https://doi.org/10.2528/pierb22052002

Kumar, V., & Park, M. (2012). A 24 GHz CMOS power amplifier using reversed body bias technique. *Science of Advanced Materials*, *4*, 1–xx. https://doi.org/10.1166/sam.2012.4567

Lee, M., Yang, J., Lee, J., & Park, C. (2024). Design techniques for wideband CMOS power amplifiers for multi-band and multi-standard wireless communications. *Electronics*, *13*(9), 1695. https://doi.org/10.3390/electronics13091695

Li, L., & Zhang, Z. (2025). A 28 GHz transformer-based doherty power amplifier for fr2 5g applications in 40 nm CMOS. *International Journal of Electronics*, *112*(3), 1–xx. https://doi.org/10.1080/00207217.2024.2312557

Liu, Z., Chen, X., Wu, H., Wang, Z., & Chen, X. (2025). Integrated sensing and edge AI: Realizing intelligent perception in 6G. *Microwave and Optical Technology Letters*. https://doi.org/10.48550/arXiv.2501.06726

Luo, J., Shen, Y., & Peng, Y. (2024). An 18–33 GHz CMOS LNA with 26.7 db peak gain and 2.8 dB minimum NF for K/Ka-band applications. *AEU – International Journal of Electronics and Communications*, *177*, 155175. https://doi.org/10.1016/j.aeue.2024.155175

Mayeda, J., Lie, D. G., & Lopez, J. (2022). Broadband millimeter-wave 5g power amplifier design in 22 nm CMOS FD-SOI and 40 nm GaN HEMT. *Electronics*, *11*(5), 683. https://doi.org/10.3390/electronics11050683

Park, M., & Kumar, V. (2021). A 3.5 GHz hybrid CMOS class E power amplifier with reverse body bias design for 5G applications. *AIP Conference Proceedings*, *2339*, 1–xx. https://doi.org/10.1063/5.0182394

Pozar, D. M. (2000). *Microwave and RF design of wireless systems*. John Wiley & Sons.

Pozgar, G., & Tarasiuk, S. (2017). Stability analysis and design guidelines for broadband amplifiers. *IET Microwaves, Antennas & Propagation*, *11*(15), 2067–2076. https://doi.org/10.1049/iet-map.2017.0456

Qualcomm. (2026). How 5G will transform industrial IoT: Private 5G networks and edge AI for next-generation automation [Qualcomm Technologies, Inc., viewed 2026]. https://www.qualcomm.com/research/5g/5g-industrial-iot

Rüddenklau, U., Geen, M., Pallotta, A., Barrett, M., Wambacq, P., & Sellars, M. (2018). *mmWave semiconductor industry technologies: Status and evolution* (2nd) [ETSI White Paper No. 15]. ETSI.

Sun, N.-Z., Gao, L., Zeng, W., Hu, J., Liu, X., & Zhang, X. Y. (2025). A balanced power amplifier with complementary adaptive bias in 28-nm bulk cmos for 5g millimeter-wave systems. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *72*(1), 1–xx. https://doi.org/10.1109/TCSII.2024.3480706

Taiwan Semiconductor Manufacturing Company (TSMC). (2026). 0.18 µm technology (logic platform) [TSMC website, viewed 26 February 2026]. https://www.tsmc.com/english/

Wang, X., Guo, B., Wu, J., & Gong, J. (2020). A 28 GHz front-end for phased array receivers simulated in 180 nm CMOS. *IEEE International Conference on Semiconductor Electronics (ICSE)*. https://doi.org/10.1016/j.asej.2023.10236

Xie, K., Wang, K., & Zhang, H. (2023). A two-way three-stage w-band power amplifier with series–parallel inductor-based t-type inter-stage matching network. *Microelectronics Journal*, *135*, 105770. https://doi.org/10.1016/j.mejo.2023.105770

Yang, Y., Mao, M., Xu, J., Liu, H., Wang, J., & Song, K. (2025). Millimeter-wave antennas for 5G wireless communications: Technologies, challenges, and future trends. *Sensors*, *25*, 5424. https://doi.org/10.3390/s25175424

Yue, P., & Rodwell, M. (2006). Mm-Wave IC design: The transition from III–V to CMOS circuit techniques [IEEE CSIC short course].

Zeng, W., Gao, L., Sun, N., Xu, H., Xue, Q., & Zhang, X. (2023). A 19.7-to-43.8-GHz power amplifier with broadband linearization technique in 28-nm bulk CMOS. *2023 IEEE International Solid-State Circuits Conference (ISSCC)*. https://doi.org/10.1109/ISSCC42615.2023.10067840

Zeng, W., Gao, L., Sun, N.-Z., Li, H.-Y., Xu, J.-X., & Xu, H. (2024). A compact 19.7- to 43.8-GHz power amplifier with 20.3-dBm Psat and 35.5% PAE in 28-nm bulk CMOS. *IEEE Journal of Solid-State Circuits*, *59*(8), 1–xx. https://doi.org/10.1109/JSSC.2024.3364096

Zhao, Y., Hou, H., Zhang, S., Wang, H., & Chang, S. (2023). A 28-GHz wideband power amplifier with dual-pole tuning superposition technique in 55-nm RF CMOS. *Integration*, *83*, 101–107. https://doi.org/10.1016/j.vlsi.2022.09.004

Zheng, W., Deng, W., Gong, J., Jia, H., Li, D., & Wu, H. (2025). A 22-to-50 GHz bi-directional beamforming CMOS front-end with distributed impedance reshaping technique for 5g nr fr2 applications. *2025 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 135–138. https://doi.org/10.1109/RFIC61188.2025.11082867