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VLSI CIRCUIT OPTIMIZATION FOR 8051 MCU

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ABSTRACT

With the aid of Electronic Design Automation tools, we perform circuit optimization on the 8051 microcontroller. The original 8051 microcontroller operates at a clock frequency 12 MHz, and it was designed based on 3.5-µm process technology. Hence, the device is slow and the chip size is large. To enhance the performance of the device and to minimize the die size, we used 90-nm technology in our design. We first performed optimization when mapping the RTL codes with the 90 nm standard cell libraries. Once the gate level netlist was generated, we developed the layout of the device by going through floor-planning, placement, and routing. We show that our new design is capable of operating at 150 MHz (i.e., 12.5 times faster than the original design), with a significant reduction in chip size (i.e., the total area is 77249.814850 μm^2). The power consumption of the chip is 593.9899 µW, which is at least 32% lower than that of other 8051 derivatives.

Keywords: Floor-planning; Physical design; Placement; Routing; Synthesis

1. INTRODUCTION

Despite being introduced by Intel more than three decades ago in 1980, the MCS-51 or better known as the 8051 microcontroller remains one of the most popular general purpose microcontrollers in use until today. Numerous vendors have developed these microcontrollers and are still releasing updates for their enhanced binary compatible 8051 derivatives. This explains the continued popularity of the device. Applications of the 8051 microcontroller encompass a wide range of technical areas, including embedded systems, robotics, and telecommunications (Chang et al., 2013; Kanniga & Sundarajan, 2015; Jain et al., 2013; Pahuja & Kumar, 2014; Arsalan, 2013).

The performance of the original Intel 8051 microcontroller, however, is relatively obsolete in today's technology. The device, for example, only operates at 8-bit with a low clock frequency of 12 MHz. Since the technology process of this device is 3.5 µm, it also has a large chip size and can therefore only be fabricated in a dual inline package (DIP). The current applications of the original 8051 microcontroller are quite restricted. It is mainly used as a teaching material in undergraduate engineering courses.

To enhance the performance of the original 8051 microcontroller, we perform Very Large Scale Integration (VLSI) circuit optimization on the device. Here, we present modification on the VLSI design of the 8051 microcontroller from its Register Transfer Language (RTL) code to its

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Graphic Database System II (GDSII) file. We demonstrate that by synthesizing the RTL codes based on an updated transistor technology and by redesigning the layout of the chip, the performance of the device (i.e., its clock frequency) can be significantly enhanced and the chip size minimized. By carefully managing the power consumption when optimizing the device, our new design requires considerably lower power in comparison with its other derivatives.

2. METHODOLOGGY

Designing a complete chip from its system specifications to its final layout is a laborious process. At the front end, the design flow involves RTL design, design verification, logic synthesis, and static timing analysis (STA), whereas at the back end, it involves floor-planning, power network synthesis (PNS), clock tree synthesis (CTS), placement and routing, chip finishing, and physical verification. Although the flow may appear routine, some of these processes are actually iterative, and therefore, they may have to be repeated more than once. This is particularly true when violations – such as timing, design rule checks (DRC), layout versus schematic (LVS) violations – are found during verifications. For our VLSI design, we implement Electronic Design Automation (EDA) tools, i.e. Design Compiler for synthesis and IC Compiler for physical design (Synopsys, 2007). Here, we illustrate in detail the essential processes applied in our circuit optimization.

2.1. Synthesis

To reduce the design turn-around-time, we obtained Intel 8051 equivalent RTL source code from Oregano Systems (2013). After compiling the RTL code and performing libraries and design checks, we synthesize the design with the 90-nm technology libraries. In the mapping process, we set the clock frequency to operate at 150 MHz and the die area to be minimum. Once the design passes all the analysis and meets all the design constraints, the gate level netlist is generated. The netlist is required in the physical design stage in order to develop the layout of the design.

2.2. Floor Planning

In the physical design, the libraries for floor planning are first set up. The core area and routing area are then defined. The core utilization ratio is set to the appropriate value in order to provide margins for routability. Once the floor plan is created, the standard cells are legally placed without any optimization. This process is known as virtual flat placement. This is done in order to analyze the impact of the floor plan on timing violations and routing congestions as well as to plan the power structure. Routing congestions usually occur when a large amount of wire nets are routed in a narrow area. The tool applies global routing methodology to check for routing congestions. In the global routing process, the tool divides the chip into global-route cells (GRCs). Each GRC consists of a finite number of routing wire. The tool then calculates the ratio of the amount of routed nets to the number of available nets in each GRC. A ratio of more than one indicates that routing congestion exists in that particular grid cell. If the congestions are found to be unacceptable, modifications are performed on the top-level pads or ports, core aspect ratio and size, as well as the power grid structure.

The last step in floor planning is power network synthesis (PNS). After the logical power and ground connections are defined, the power rails along the standard cell placement rows are created. The current and resistance or IR drop map is then used to analyze the power network.

2.3. Placement and Routing

Once the design passes the PNS test, it is ready for placement. At this stage, the EDA tool performs area, power, and timing optimizations and also clock tree synthesis (CTS) on the design. Timing and congestion are subsequently analyzed to check for violations. If violations are found, the path grouping approach is typically applied at the affected areas. After those

paths are grouped based on the clocks, which control their endpoints, optimizations and CTS are performed again. This process will be repeated until all violations are solved. The incremental-timing-driven logic optimization, with placement legalization, is used to perform final placement on the design.

Once placement is completed, the tool performs global routing for the initial routing. This is followed by detailed routing and optimization. DRC violations are commonly detected at this stage. Some of these violations could be fixed by running the Engineering Change Order (ECO) route. Resolving others, such as those that involve spacing issues, may not be as straightforward. Very often, we may have to revert back to floor planning again to resolve the violations. Hence, these two processes – floor planning and placement and routing – would have to be executed in an iterative manner.

2.4. Physical Verification

At the final design stage, LVS is performed to compare the physical layout with the optimized gate level netlist. This is to ensure that the logical descriptions of the design are not altered during the physical implementation process. Some final verifications, such as CTS and final area analysis, are conducted before streaming out the GDSII file. The GDSII file is necessary for fabricating the chip.

3. RESULTS AND DISCUSSION

Figure 1 shows the initial floor plan created by the EDA tool. The little boxes in pink are the standard cells, while the green box in the leftmost of the figure denotes the terminals meant for the input and output (I/O) ports. The design consists of 5574 standard cells. The core utilization area is around 0.8. This means that 80% of the area is available for standard cells, macros, and blockage placement. The remaining 20% of the area is reserved for routing. The gap between the terminals and the core area is about 10 µm.

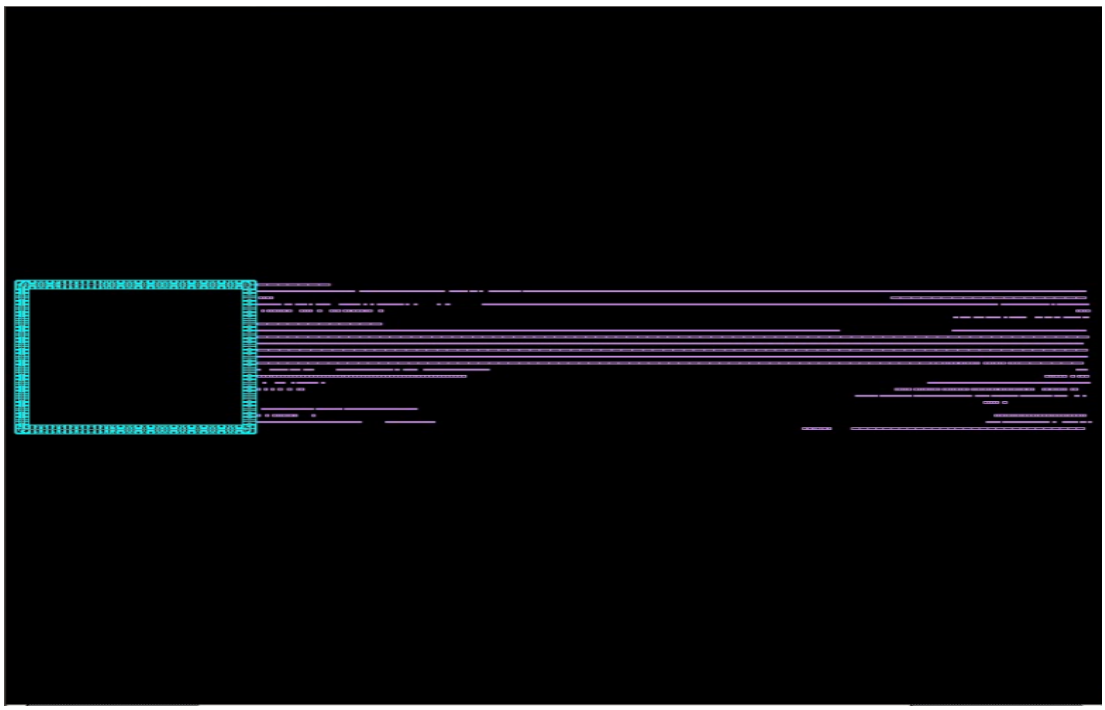

Figure 1 Floor plan of the proposed 8051 microcontroller

Figure 2 shows the virtual placement, which was created to check for routing congestions and timing violations. As can be observed from Figure 3, the virtual placement report indicates that

the total number of cells violating the core area is zero. Thus, no violations are detected and all cells can be placed into the core area, i.e., 80% of the total design area.

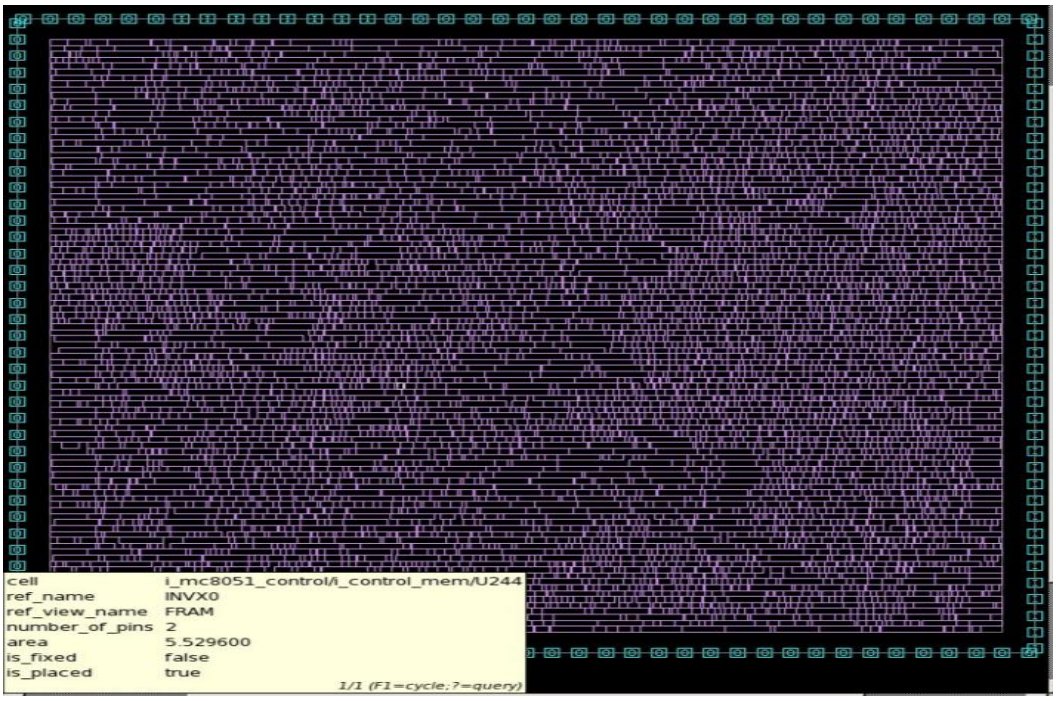

Figure 2 Virtual placement for the proposed 8051 microcontroller

```
Number of cells violating core area: 0
Total number of cells violating plan group or core area: 0
*** global placement done.
```

Figure 3 Virtual placement report

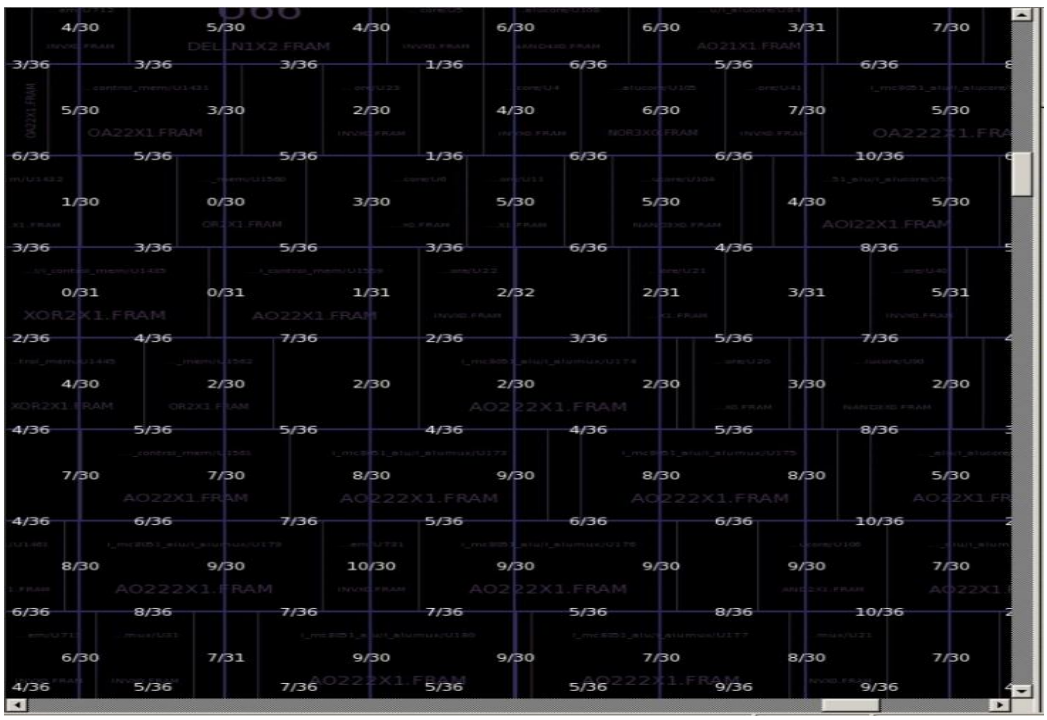

Figure 4 Congestion map with GRCs

A portion of the congestion heat map is shown in Figure 4. The congestion heat map is used to visualize the severity of congestion in the global route cells (GRCs). As mentioned in the previous section, the EDA tool calculates the ratio of the amount of routed nets to the number of available nets in each GRC. As can be seen from Figure 4, the ratios in the GRCs are less than one. The result suggests that there is no congestion in that particular portion. A summary of the congestion report is shown in Figure 5. From the report, we can see that the total number of GRCs is 10100, and none of them experience overflows. In other words, there is no routing congestion in the design.

```
++++++++++++++++++++++++++++++++++++++++++++++++
 Overall Congestion Map Data:
++++++++++++++++++++++++++++++++++++++++++++++++
There are 10100 GRCs (Global Route Cell) in this design
************************************************************
****************** GRC based congestion report *****************
************************************************************
  0 GRCs with overflow: 0 with H overflow and 0 with V overflow
```

Figure 5 Congestion report

The top hierarchical view of the final layout after routing and verifications and a close view of the center of the layout are shown in Figures 6 and 7, respectively. The design is routed with nine metal layers. The bottom level consists of the standard cells. The metal fillers and filler cells are inserted into the design to resolve the density violations.

Figure 8 shows the final power report of the device. The total power consumption is 593.9899 µW. As compared to the power consumptions of the 8051 derivatives reported in the literature (Saponara et al., 2004; Iozzi et al., 2005; Li et al., 2009; Sai & Mickle, 2013), the optimized 8051 microcontrolled we designed requires at least 1.46 times less power to operate. In other words, power consumption has been reduced by at least 32%. The feature size of the transistors implemented in our design is almost 40 times smaller than in the original design.

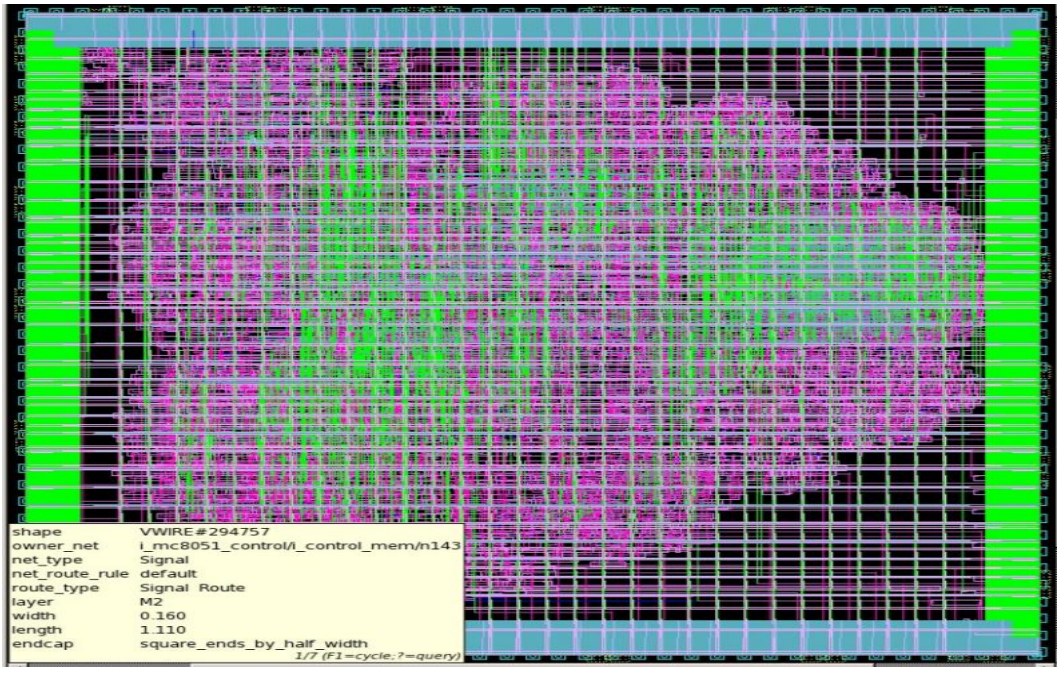

Figure 6 Final layout

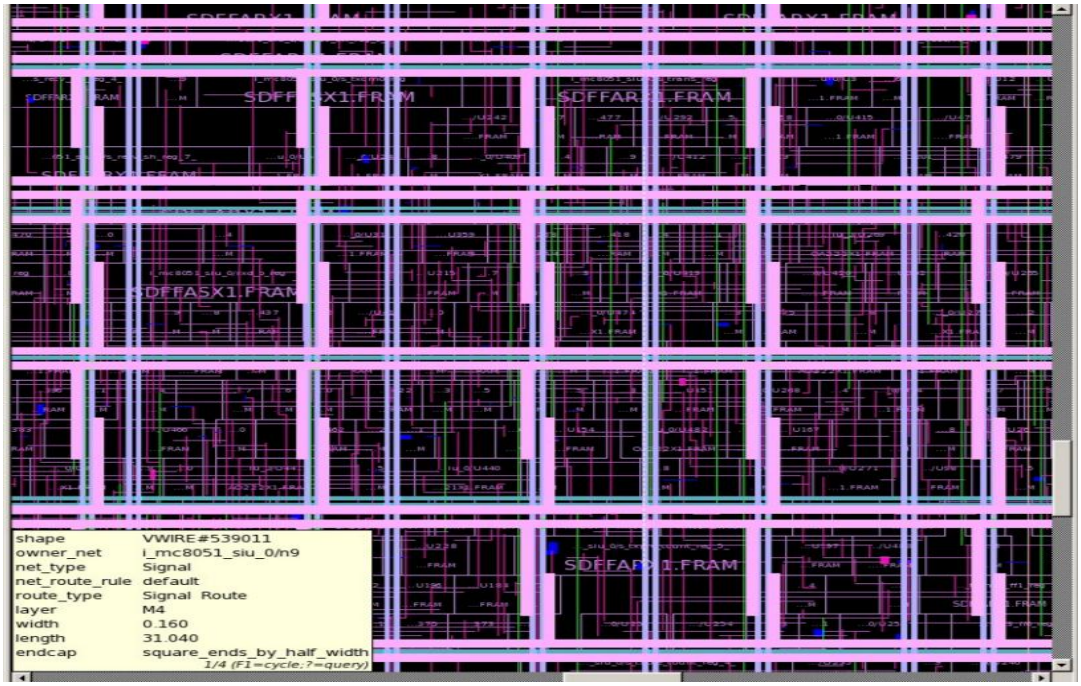

Figure 7 Centre of the layout

The significant reduction in the effective channel length allows for an increase in the switching speed of the logic components (Sung et al., 1998) and less power required to turn on the transistors. Further, the same number of transistors could be fabricated in a die with a smaller size (Ahmad et al., 2006). By optimizing the microcontroller using the 90-nm technology library, we show that our design can help save much energy, apart from operating at a faster speed and having a smaller chip size. It is interesting to find that the power consumption in our device using the 90-nm process technology is lower than in the device using the 45 nm process technology (Sai & Mickle, 2013). We attribute this phenomenon to the careful planning performed during floor planning and placement and routing. By carefully placing the cells and optimizing the routing process, power consumption of the chip can be minimized.

```
  Cell Internal Power  = 143.1559 uW   (36%)
  Net Switching Power  = 256.6308 uW   (64%)
                         ---------
Total Dynamic Power    = 399.7867 uW  (100%)

Cell Leakage Power     = 194.2029 uW


                 Internal         Switching           Leakage             Total
Power Group      Power            Power               Power               Power   (   %    )  Attrs
--------------------------------------------------------------------------------------------------
io_pad             0.0000           0.0000              0.0000              0.0000  (   0.00%)
memory             0.0000           0.0000              0.0000              0.0000  (   0.00%)
black_box          0.0000           0.0000              0.0000              0.0000  (   0.00%)
clock_network     38.9558         127.7010           1.2949e+06          167.9517  (  28.28%)
register          11.8236           8.3318           5.0552e+07           70.7075  (  11.90%)
sequential         0.0000           0.0000              0.0000              0.0000  (   0.00%)
combinational     92.3768         120.5980           1.4236e+08          355.3307  (  59.82%)
--------------------------------------------------------------------------------------------------
Total           143.1562 uW      256.6307 uW      1.9420e+08 pW       593.9899 uW
```

Figure 8 Final power report

Table 1 Comparison of the design before and after optimization

	Before Optimization	After Optimization
Clock Frequency	12 MHz	150 MHz
Area	104984.540474 μm^2 (Based on saed90nm_max library)	77249.814850 μm^2

4. CONCLUSION

In this paper, we have shown that the design of the original 8051 microcontroller can be significantly enhanced. By synthesizing the RTL code using libraries with the technology size half of its original and by carefully designing its VLSI layout with the aid of Synopsys EDA tools, we were able to increase the clock frequency to 150 MHz and reduce the die size to 77249.814850 μm^2. The power consumption of our chip is 593.9899 μW, which is found to be at least 32% lower than that of the existing 8051 derivatives.

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