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DUAL MATERIAL PILE GATE APPROACH FOR LOW LEAKAGE FINFET

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ABSTRACT

FinFET (Fin Field-Effect Transistor) technology has recently seen a major increase in adoption for use in integrated circuits because of its high immunity to short channel effects and its further ability to scale down. Previously, a major research contribution was made to reduce the leakage current in the conventional bulk devices. So many different alternatives like bulk isolation and oxide isolation are all having some pros and cons. Here in this paper, we present a novel pile gate FinFET structure to reduce the leakage current, as compared with Bulk FinFET without using any pstop implant or isolation oxide as in the Silicon-on-Insulator (SOI). The major advantage of this type of structure is that there is no need of high substrate doping, a 100% reduction in the random dopant fluctuation (RDF) and an increase in the I_{ON}/I_{OFF} value. It can be very useful to improve the drain-induced barrier lowering (DIBL) at smaller technological nodes. All the work is supported by 3D TCAD simulations, using Cogenda TCAD.

Keywords: Bulk FinFET; Charge accumulation; Leakage current; Lower doping; Pile Gate FinFET

1. INTRODUCTION

Previously, the double-gate MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor) was considered to be the most attractive device to succeed the planar CMOS (Complementary Metal-Oxide Semiconductor) transistor, (i.e., bulk mos (metal-oxide semiconductor) transistor), especially when the latter could not be scaled down any further. We need to find new ways to continue the scaling trend downwards. FinFET technology had been conceived as a result of the tremendous increase in the levels of integration (Colinge, 2007). The FinFET technology ensured a capacity to deliver superior levels of scalability needed to make sure that the current progress with increased levels of integration within integrated circuits could be maintained (Bin et al., 2002; Yoshida et al., 2005). The first successful concept of FinFET was proposed in 1999 (Huang et al., 1999) which was basically designed to reduce the short channel effects. Later, this structural design of FinFET offerred many advantages in terms of sub-threshold performance and also in IC processing. Only then, it was adopted as a major way forward for incorporation within IC technology (Moshgelani et al., 2012).

Over the years, there were several changes that FinFET had adopted, such as structures with underlap and overlap regions as reported in various researches (Pal et al., 2013; Pal et al., 2015), and those structures with different gate materials as reported in (Hussain et al., 2010), in relation to the Fin shape and so on. Gate-all-around (GAA) FinFET is one of the most recent developments in the FinFET series having the channel surrounded from all four sides (Singh et al.,

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2008). Although the main idea behind the development of FinFETs and all other structures is to reduce the short channel effects (Xu et al., 2015), this continues to be the case with scaling laws. As the device size reduces, the short channel effects are increased in bulk MOS (Metal-Oxide Semiconductor) technology, such as in the source/drain (S/D) parasidic resistance effect and/or unwanted parasitic effects, which may cause limitations in high-speed applications (Su & Li, 2015). Previously, several solutions were proposed, such as silicon-on-insulator (SOI)-based FinFET structures and sandwiching channel stop implants (pstop). In the case of NMOS (n-channel MOSFET), to reduce the leakage current, there are a few options (Colinge, 2007). Since, as the device size reduces, there is an increase in the doping levels of the device in all regions to maintain the magnitudes of the fields inside the channel, the results in threshold voltage increase. To reduce the threshold voltage, scaling in the gate oxide thickness is required. With silicon dioxide, the thickness of gate oxide is so small that it can barely produce a gate current. So the use of High-K material as a gate oxide is preferred. Also with high doping unwanted random dopant fluctuation (RDF) was reported by Asenov et al. (2001), (which was located in the bulk as well as inside the inversion layer). RDF in the channel region can alter the transistor's properties, especially the threshold voltage (Asenov, 1998). There were several solutions proposed in the previous years to lower the random dopant fluctuation (RDF), such as the use of channel underlap techniques and source/drain extension. Although FinFET, which is a non-planar technology (i.e source, drain and gate are not in the same plane as they are in the bulk planner MOSFET), it seems to be adequate for the next few years, but it is still prone to shrinking in the transistors area, where there are a few unavoidable effects, which may arise and hence the effort to reduce the short channel effects (SCE) in the Bulk FinFET is required. Several studies show that drain-induced barrier lowering (DIBL) plays an important role contributing in SCE in ultra-small channel transistors. Also, leakage is always more at the interface due to several interface charges and scattering mechanisms. According to Roy et al. (2003), the maximum part of the leakage current exists just down under the fin area in the substrate. This situation is due to less control of the gate, which is a major cause of off-state leakage (i.e., when the gate voltage is zero).

In this study, we propose a new device structure for leakage suppression using a pile gate with a different work function in the bottom gate electrode. The idea behind designing this structure is to make the lower portion of the channel (Interface between substrate and fin near source and drain) in such a way that leakage through the substrate just below the fins can be reduced. It also helps in reducing source drain punch through at lower dimensions. The main advantage of this structure is there is no need for an additional substrate doping as suggested by Liao et al. (2011), since high substrate doping results in RDF and in the case there is no buried oxide (as in the case of the Silicon-on-Insulator, SOI technology is complex and expensive). Also, deposition of oxide is not as easy as in other materials (such as *Gallium Arsenide,* GaAs) as it is in silicon because the oxide can cause problems like surface damage. So, this technique can be used with different materials, other than silicon, since there is no need of oxide deposition to reduce leakage.

2. DEVICE STRUCTURE

The device structure has been made with 3-D TCAD Tool Cogenda Genius. The device dimensions are shown in Table 1.

Table 1 Device Simulation Parameters

Parameters	Values
Silicon Fin width (W_{fin})	5 nm
Silicon Fin height (H_{fin})	15 nm
Effective Oxide thickness (EOT)	0.5 nm
Top-Gate work function	4.3 eV
Bottom-Gate work function($W.F_{bot}$)	4.9–5.19 eV
Channel length (L_g)	12 nm
Channel doping N_{ch}	5×10^{17}–5×10^{18} cm^{-3}
Source/drain doping($N_{S/D}$)	1×10^{20} cm^{-3}

The Bulk FinFET with a channel length of 12 nm, fin width of 5 nm, power supply of 0.75V at saturation region and 0.05V at the linear region is used. Both the bulk and pile-gate devices are simulated and optimized for different parameters, such as channel doping, the height of bottom gate, number of fins, etc. The variation of the bottom gate height plays an important role in off-state leakage and hence an exhaustive study of bottom gate height for optimum results is conducted. Also, we have used a small amount of isolation oxide to avoid any kind of fin inversion in the substrate part. HfO_2 (High K dielectric) is used as a gate oxide material to reduce gate leakage, which also results in the reduction in off-state leakage current. Calibration of TCAD tool is done properly before the simulations. A density gradient-based quantization model is incorporated in the simulation to account for quantum effects because of very narrow fin width. In addition the Lombardi unified mobility model is used to accommodate the acoustic phonon component as well as the surface roughness component to cover the scattering effects (Cogenda, 2010). Figure 1a shows the conventional bulk FinFET structure and the Figure 1b shows the pile gate approach used in this work.

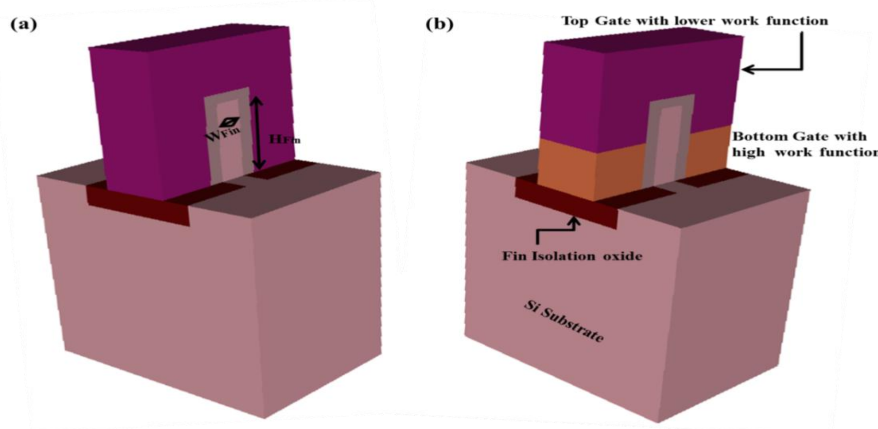

Figure 1 Middle Section of: (a) Conventional Bulk FinFET; and (b) Bulk FinFET with Pile gate approach

To avoid the Fin Inversion in the substrate we have used SiO_2 as an isolation oxide between the substrate and the bottom gate electrode as shown in Figure 1(b).

3. RESULTS

Through 3-D device modeling using Cogenda TCAD, simulations were carried out to assess the relative performance benefits of the Pile gate FinFET over the conventional Bulk FinFET shown in Figures 1a and 1b. The channel length is 12nm based on ITRS 2013(2013 ITRS). The width of the fin is taken as 5 nm and height is 15 nm. The larger fin height is taken such that it

can handle more current in it and also with larger fin height heating issues are less.

To meet the better performance substrate, doping is taken as 1×10^{16} cm^{-3}. With this specification, the leakage current is keeping the Gate voltage at zero ((i.e V_{GS}=0V) and drain voltage is varying, since it was obtained in the case of Bulk FinFET (Figure 1a) as 843 pA for V_{DS} =0.05V and 14 nA for V_{DS} =0.75V.

With the same specification, obtained results for the pile gate FinFET (Figure 1b) is much better as the leakage current was obtained as 51 pA for V_{DS} =0.05V and 124 pA for V_{DS} = 0.75V. Also to obtain the desirable threshold, the voltage top gate work-function is taken as 4.3 eV and the bottom gate work-function is taken as a varying parameter to test the performance of the device.

Figure 2 and Figure 3 show the drain current versus gate voltage plots for the bulk and pile gate FinFET, respectively. It can be seen that I_{OFF} is less in the case of pile gate FinFET which results in the higher value of I_{ON}/I_{OFF} value.

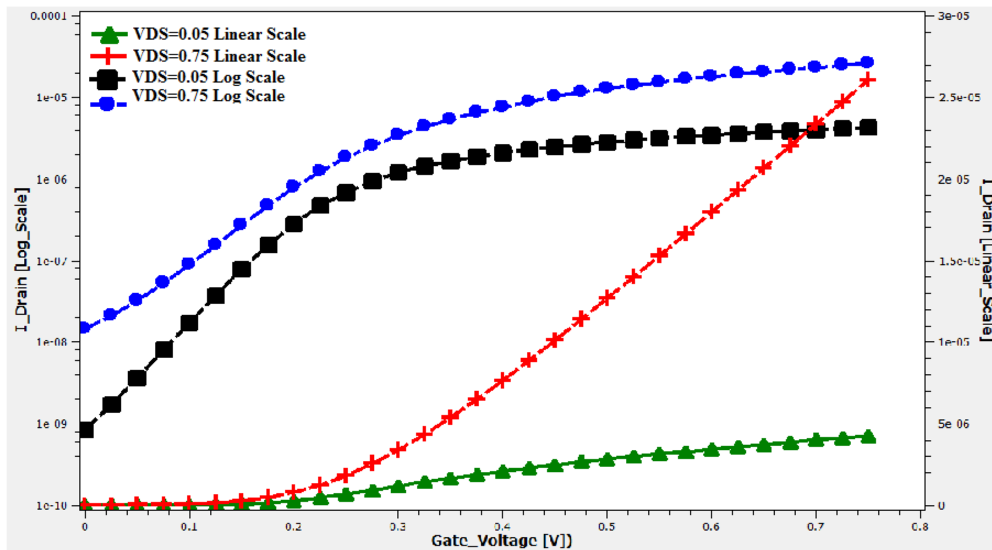

Figure 2 Obtained I_{DS}–V_{GS} characteristics for Bulk-Si FinFET in the linear and saturation region

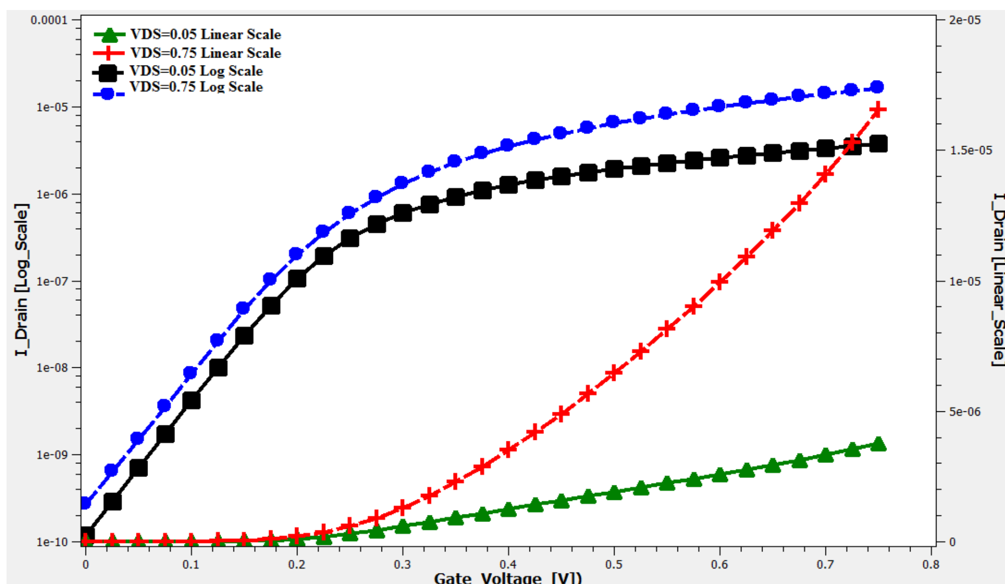

Figure 3 Obtained I_{DS}–V_{GS} characteristics for Pile-gate FinFET in the linear and saturation region

This happens because in the pile gate FinFET, the bottom gate work function is very much higher than the top gate, so for the applied gate bias, the bottom part of the fin near the fin-substrate interface seems to remain in the accumulation, causing leakage and also due to the higher work-function bottom gate, the surface potential of the area near the channel and substrate increases. Therefore, the potential barrier for the electrons causes the leakage under the channel, so higher barrier height electrons find it difficult to move from source to drain and thus it helps in suppressing drain-induced barrier lowering (DIBL).

Another advantage of this structure is with a higher work-function metal as the bottom gate and the high-k dielectric as the gate oxide. Therefore, there is a significant reduction in the gate to source-drain extension (SDE) tunneling, which ultimately reduces the off-state leakage. The other advantage of the pile gate structure is that the area just below the fin is accumulated at higher drain voltages and thus the excess charge carrier near the substrate region reduces and thus leakage through the substrate, i.e. substrate current, reduces

Conventional Bulk FinFET with a low substrate doping (1×10^{16} cm^{-3}) is used in our study of DIBL at 71mV/V. Meanwhile, the high channel and substrate doping is used to reduce the off-state leakage current to improve the performance of the Bulk FinFET. But the major drawback of the increased doping is random dopant fluctuation (RDF) effects and it will result in significant mobility degradation, scattering issues, and high parasitic capacitances. The DIBL value for the pile gate FinFET with a 9 nm bottom gate height and 5×10^{18} cm^{-3} channel doping is found to be 63mV/V. It can be seen that with a lower DIBL value, the pile gate FinFET can help in reduction of threshold voltage fluctuation.

To further increase the I_{on} (at $V_{GS}=V_{DD}$), we increased the number of fins on the same substrate. With two fins, the obtained Ion is nearly three times that of with a single fin. The drain current versus gate voltage plot is shown in Figure 4 and the comparison of I_{ON} and I_{OFF} is shown in Table 2.

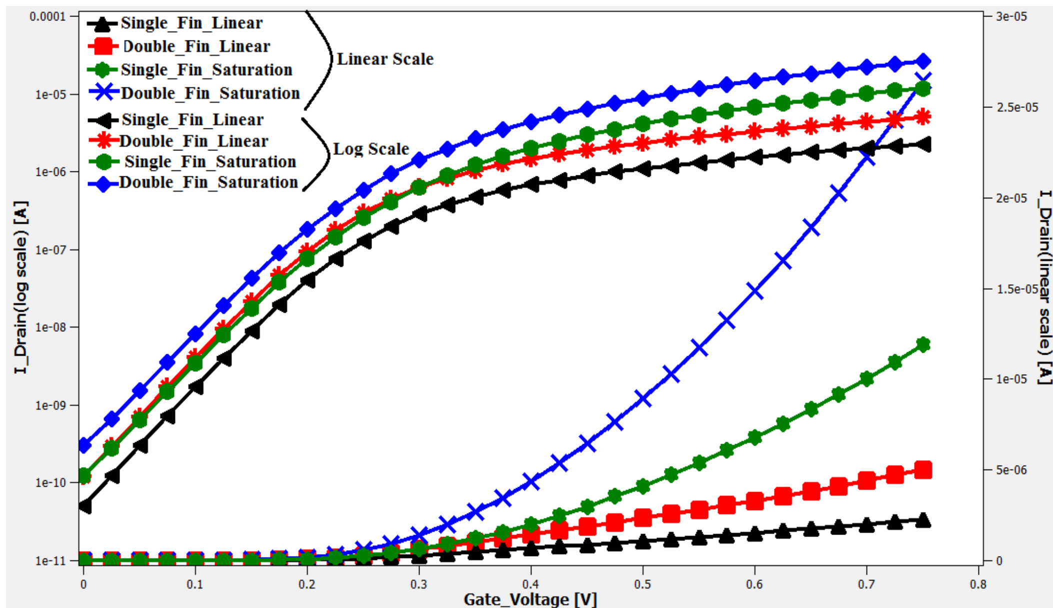

Figure 4 Obtained I_{DS}–V_{GS} characteristics for Pile-gate FinFET with single and double Fins in the linear and saturation region with both linear and log axis

3.1. Effect of The Bottom Gate Height and Work-Function on Leakage Currents

Leakage currents can be reduced by increasing the bottom gate height. Table 3 shows the leakage current with different heights for the bottom gate. It is clear as the height of the bottom

gate increases, the barrier height for the electrons to transfer from source to drain increases. Thus, the leakage current reduces because the larger area near the fin-substrate interface is accumulated.

Table 2 I_{ON}/I_{OFF} for single and double fin

Parameters	Single Fin	Double Fin
I_{ON}(linear, saturation)	2.3 uA, 11 uA	6.3 uA, 26 uA
I_{ON}/I_{OFF} (Linear)	44000	56000
I_{ON}/I_{OFF} (Saturation)	91000	95000

Table 3 Leakage current for different bottom gate heights

Bottom gate Thickness	Leakage Current (A)
5 nm	1.485×10^{10}
7 nm	8.889×10^{11}
9 nm	5.127×10^{11}
11 nm	1.594×10^{11}

Figure 5 shows the OFF current variation with the bottom gate height. The higher the bottom gate height, lower is the OFF current. The ON current is also reduced with an increase in the bottom gate height, but overall the I_{ON}/I_{OFF} increases.

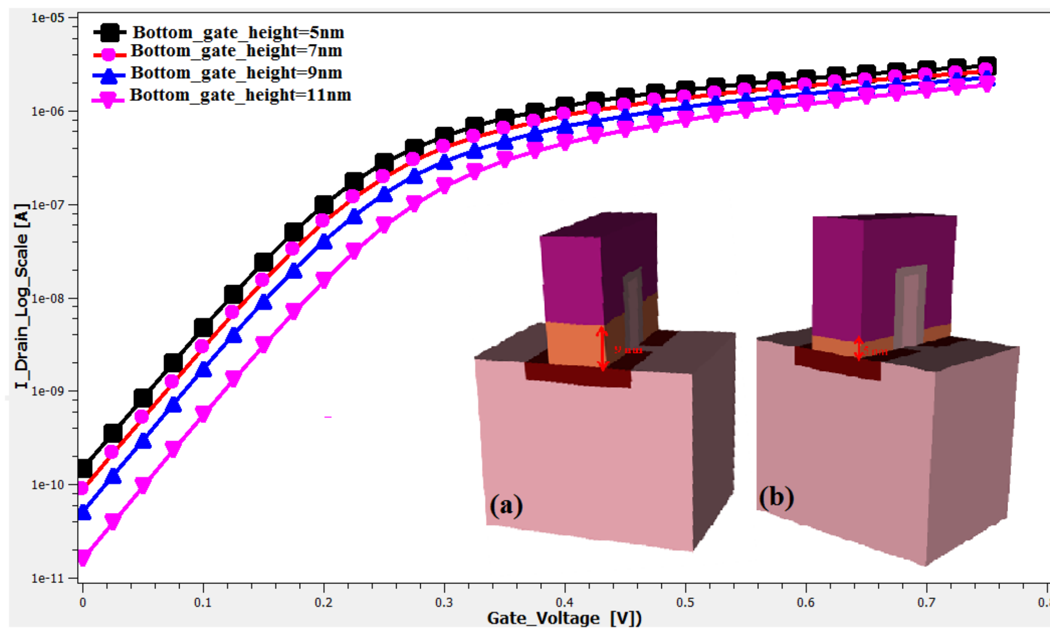

Figure 5 Obtained I_{DS}–V_{GS} (Log scale) characteristics for Pile-gate FinFET with different heights shown for the bottom gate: (a) Bottom gate with 9nm height; (b) Bottom gate with 5nm height

Another way to reduce the leakage is to increase the work function of the bottom gate. The simulation results show that with 9 nm bottom gate thickness for three different work function values of the bottom gate, i.e. 4.9eV, 5.1eV and 5.2eV, the obtained leakage current is 51pA, 36pA and 30pA, respectively. But while choosing the work function, we have to maintain the highest I_{ON}/I_{OFF}. So a trade-off can be made between leakage current and I_{ON}/I_{OFF}. In this way

we can tune the device leakage by changing the work-function and height of the bottom gate electrode to obtain the maximum I_{ON}/I_{OFF}. Figure 6 shows the DIBL and I_{ON}/I_{OFF} as a function of channel doping (N_{ch}) for two different heights of the bottom gate. In the case of the Pile gate, (FinFET) the effect of drain-induced lowering is lower as compared to the Bulk FinFET because at the higher drain voltage, there is also the source energy barrier for the charge carrier which remains intact, resulting in lower sub-threshold leakage and lower threshold voltage fluctuation. just as we increased the drain voltage. Also, from Figure 6 it can be seen that the 9 nm bottom gate thickness is at a position of higher doping and the I_{ON}/I_{OFF} ratio is maximum because the drain on the current primarily depends upon the top part of the fin and bottom part, which is responsible for leakage. Where the effect of gate is less, in so incorporating the pile gate approach we reduce the OFF current, while maintaining the required ON current.

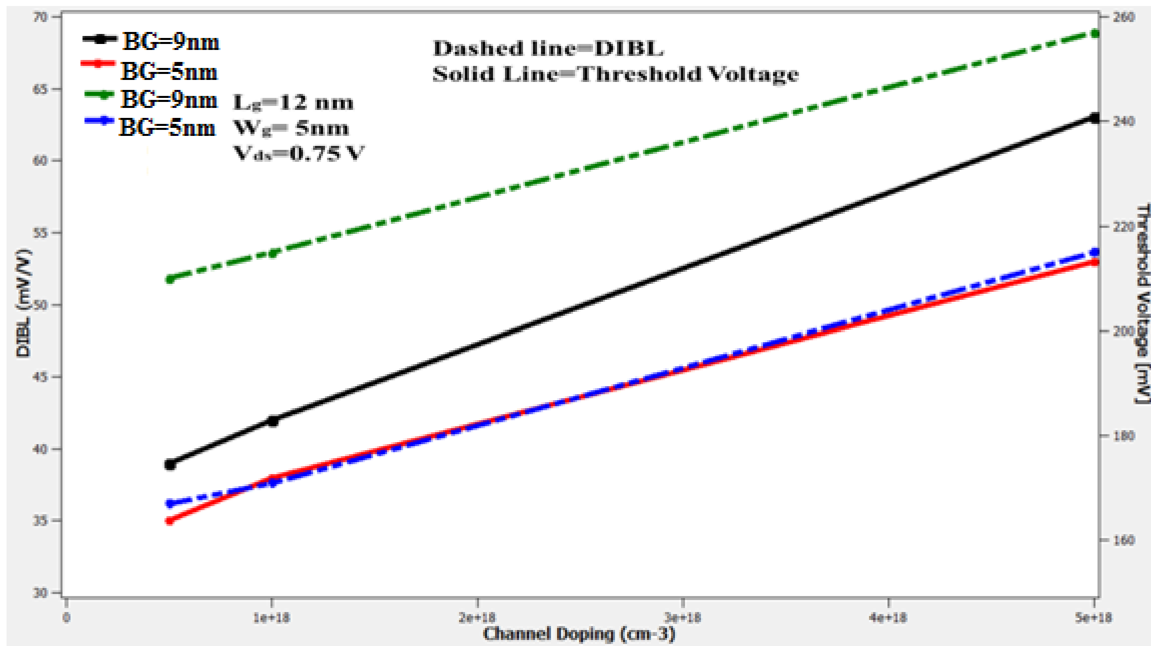

Figure 6 DIBL and threshold voltage as a function of channel doping (N_{CH}) for different heights of the bottom gate

Table 4 shows the sub-threshold slope for two different bottom gate heights as a function of channel doping. A very steep sub-threshold slope device can be turned on- and turned off- very fast. With 9 nm bottom gate height and 5×10^{17} cm^{-3} doping, the sub-threshold slope is almost near to its theoretical possible limits, i.e., 60 mV/dec.

Table 4 Sub-threshold slope as a function of channel doping for two different bottom gate heights

Channel doping (cm^{-3})	SS (mV/dec) / Linear(9 nm, 5 nm)	SS (mV/dec) / Saturation(9 nm, 5nm)
5×10^{17}	63.92 / 64.49	65.76 / 66.02
1×10^{18}	64.15 / 64.80	66.08 / 66.34
5×10^{18}	64.77 / 65.52	67.97 / 68.01

4. CONCLUSION

We have presented the unique advantages of a pile gate FinFET over conventional Bulk

FinFET for low leakage usage needed in future applications, such as mobiles. By incorporating the bottom gate with the high work-function, the pile gate FinFET can achieve less leakage current compared to the Bulk FinFET and still have an improved I_{ON}/I_{OFF}. With the high work-function of the bottom gate, the area near the substrate-channel has a high surface potential, which increases the barrier height for the electrons. This condition causes the leakage current near the interface. This structure can be implemented at a very much lower technological node because the DIBL is no longer a problem for designing, thus it increases the I_{ON}/I_{OFF} ratio. The other main advantage of this technique is that there is no requirement of high doping for leakage reduction, thus reducing the RDF. Also, the technology is compatible with the present CMOS process and therefore, there is no need to change the process technology.

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