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THE DESIGN OF A HIGH SPEED NONLINEAR FEEDBACK-BASED CURRENT COMPARATOR

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ABSTRACT

In this paper a new current comparator architecture is presented, which utilizes the concept of nonlinear feedback to speed up the operation. The analytical formulation for quantifying the effect of the feedback is put forward. The functionality of the proposed comparator is verified using simulations carried out on an Orcad Pspice tool using Taiwan Semiconductors Manufacturing Company (TSMC) 0.18 µm technology parameters. The resolution and delay are found to be ± 10 nA and 1.48 ns, respectively at a reference current of 1µA. The effects of parameter variations on the performance of the proposed comparator at different design corners is also studied. The usefulness of the proposed comparator is demonstrated through a 3-bit current mode flash Analog to Digital Converter (ADC) and its performance parameters are also calculated using simulations. The simulation results show that the 3-bit current mode flash Analog to Digital Converter exhibits no missing codes and has Differential Non-Linearity (DNL) of -0.25 Least Significant Bit (LSB) and Integral Non-Linearity (INL) of -0.19 LSB.

Keywords: Current comparator; Current mode analog to digital converters; High resolution; Nonlinear feedback

1. INTRODUCTION

Amplitude comparison of signals is an essential operation in numerous applications, such as front end signal processing, Very Large Scale Integration (VLSI) neural network, quiescent supply current (IDDQ) testing, neuromorphic systems etc., (Banks et al., 2005). The overall performance of these systems depends heavily on comparator, therefore the desired features of comparator is high speed and accuracy and low power dissipation. The current comparator has received considerable attention as many sensors in System on Chip (SoC), such as temperature, Complementary Metal-Oxide Semiconductor (CMOS), Advanced Photo System (APS), etc., provide an output current signal. The current signals can be directly processed by current comparators whereas voltage comparator would require a current to voltage converters and therefore current comparator saves crucial power and area.

The current comparator provides a voltage output using a process which involves injection of two currents and distinguishing whether the difference of two currents is positive or negative. The design of current comparators has to be done keeping the need for low input impedance, quick time response and accuracy in focus. A number of current comparators are available

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in literature which can broadly be classified on the basis of current sensing mechanism (Toumazou et al., 1990; Freitas & Current, 1993; Traff, 1992; Banks & Toumazou, 2008; Chen et al., 2001; Tang & Toumazou, 1994; Min & Kim, 1998; Ravezzi et al., 1997; Tang & Pun, 2009; Chavoshisani & Hashemipor, 2011). The first generation current comparators are based on sensing input current at a low impedance node followed by a voltage amplification mechanism (Frietas et al., 1993). This technique is known as a resistive input scheme. It has limited resolution and operational frequency. The input current sensing mechanism is capacitive in the second generation current comparators. This technique provides better resolution than that reported in Frietas et al., (1993) due to the larger voltage swing at input node, but it still suffers from low-speed characteristics. A remedy to these limitations was reported by Traff, (1992), where nonlinear feedback is introduced along with capacitive sensing, which lowers the input impedance and provides better speed. Subsequently, many structures based on concept of Traff, (1992) have been reported in various researches, (Banks et al., 2008; Chen et al., 2001; Tang et al., 1994; Min et al., 1998; Ravezzi et al., 1997; Tang et al., 2009; Chavoshisani & Hashemipor, 2011) as an improvement over it. The comparators reported in Chavoshisani and Hashemipor (2011) are also based on capacitive sensing, but employ active elements, such as a current conveyor, second generation (CCII) (Chavoshisani & Hashemipor, 2011) and a differential current conveyor, second generation (DCCII) as reported by Chavoshisani et al., (2011). As these structures accept the difference of input currents, an additional current subtraction circuit is required for complete comparison, which will cause the variation in the reported performance parameters. (Traff, 1992; Banks et al., 2008; Chen et al., 2001; Tang & Toumazou, 1994; Min & Kim, 1998; Ravezzi et al., 1997; Tang & Pun, 2009; Chavoshisani & Hashemipor, 2011). In this paper, a current comparator is proposed that has an inbuilt current differencing circuitry. It uses three stage resistive load amplifiers in the gain stage and a nonlinear feedback to reduce impedance and voltage swing at an input node, which leads to improvement in the speed and resolution of the comparator. A CMOS inverter is used as output stage to provide rail-to-rail swing for lower currents.

The paper is organized as follows: the proposed current comparator architecture along with analytical formulation to quantify the effect of feedback on the current comparator performance is presented. The performance of the theoretical proposition is verified through Pspice simulations using TSMC 0.18µm CMOS technology parameters. An application of the proposed current comparator is demonstrated by implementing a three bit current mode flash ADC. The functionality of the same is verified through simulations and performance parameters are calculated. Finally, conclusions are drawn.

2. CURRENT COMPARATOR

A current comparator compares an input current with a reference current and gives an output voltage. The concept of current comparator is reported by Traff, (1992), as shown in Figure 1. The current Iin shown in Figure 1 is the difference between input and reference currents. The output (Vout) is high when the input current is positive and vice versa. However, in general, a current comparator consists of a current difference stage, a gain stage followed by an output stage as reported by Chavoshisani et al., (2011) and depicted in Figure 2.

The architecture of the proposed comparator is illustrated in Figure 3 in which transistors Mc1-Mc12 form the current differencing stage, which provides output current I_{diff} as the difference of I_{in1} and I_{in2}. The gain stage of the proposed comparator consists of three resistive load amplifier cascaded stages (M1-M4, M2-M5, M3-M6), respectively and a nonlinear feedback (Mpf - Mnf) around the gain stage for performance improvement. The type of nonlinear feedback is of a shunt-shunt type i.e., output voltage is sampled and fed to the input in the form of current. This is achieved by connecting the output node C to the gates of the feedback

transistors (Mpf-Mnf), while tying their sources to input node B. The output stage (Mz1-Mz2) provides rail-to-rail swing even under low input current differences.

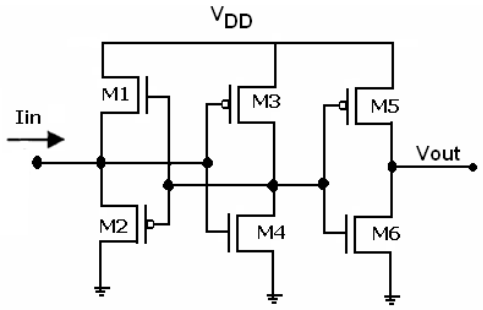


Figure 1 Current comparator concept (Traff, 1992)

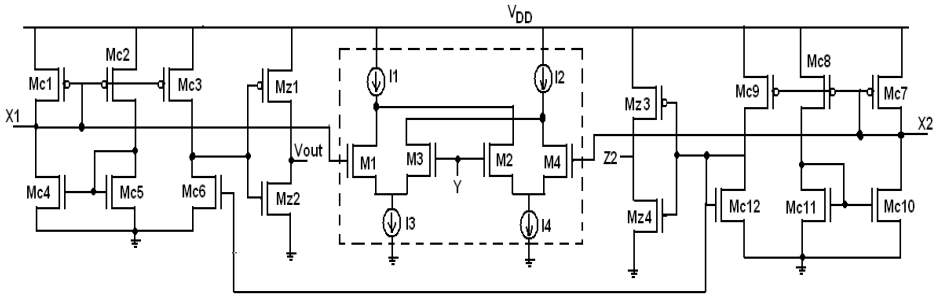


Figure 2 Differential current conveyor based current comparator (Chavoshisani et. al, 2011)

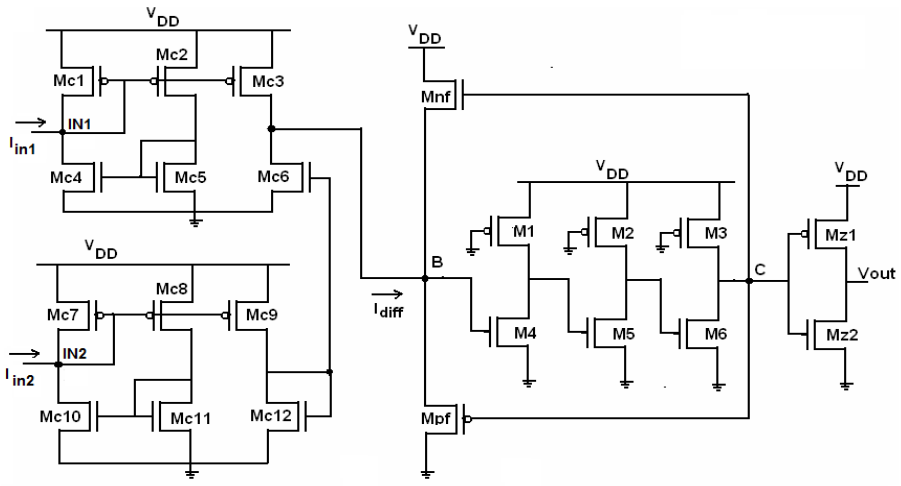


Figure 3 Proposed current comparator

The input impedance R_{in1} and R_{in2} of the terminals IN1 and IN2 are as shown in Equation 1:

$$R_{in1} = \frac{1}{g_{mc1}} \| r_{oc1} \| r_{oc4}$$
$$R_{in2} = \frac{1}{g_{mc7}} \| r_{oc7} \| r_{oc10} \quad (1)$$

where g_{mci} and r_{oci} are transconductance and output resistances of transistors Mci.

The overall operation of the nonlinear feedback is explained as follows: For low current

differences the transistors Mpf and Mnf do not turn ON. Thus the node B impedance is capacitive, which causes slow charging/ discharging of the node voltage to which the gain and the output stages respond. For high positive values of current I_{diff}, node B voltage increases, which results in a reduction in node C voltage, due to inverting nature of the cascaded amplifier stage. The transistor Mpf switches ON as its source (node B) and gate (node C) voltages are respectively high and low. Conversely, the high negative values of current I_{diff} cause a decrease in node B voltage and a subsequent increase in node C voltage. This makes Mnf ON, due to a low voltage at its source (node B) and a high voltage at its gate (node C). For high values of current I_{diff} the impedance of node B turns resistive. Thus, the circuit responds to a wide range of input difference currents. Further, nonlinear feedback helps in reducing the voltage swing and input impedance at node B, as discussed in the following section.

2.1. Voltage Swing Reduction

An expression for voltage swing is formulated in this subsection. The source voltage of Mpf and Mnf (node B) for positive and negative input current differences is given respectively as shown in Equations 2 and 3:

$$V_{B+} = \frac{A_{OL}}{1+A_{OL}} V_Q + \frac{1}{1+A_{OL}} |V_{TP}| \tag{2}$$

$$V_{B-} = \frac{A_{OL}}{1+A_{OL}} V_Q - \frac{1}{1+A_{OL}} V_{TN} \tag{3}$$

where V_Q refers to Q-point voltage of the first amplifier (M1-M4) of the cascaded amplifier stage, V_{TP}, V_{TN} are the threshold voltage of the PMOS and NMOS transistors respectively and A_{OL} represents the overall open loop gain of the cascaded amplifier stages.

It may be noted from Equation 2 and Equation 3 that the voltage swing of the input node B (V_{B+} - V_{B-}) is reduced, due to nonlinear feedback. The smaller swing leads to faster charging/discharging of node B and speeds up the response time.

The overall open loop gain of the cascaded amplifier stages is given by Equation 4:

$$A_{OL} = \frac{A_{O1}}{1+sR_1C_1} \cdot \frac{A_{O2}}{1+sR_2C_2} \cdot \frac{A_{O3}}{1+sR_3C_3} \tag{4}$$

where $A_{Oi,}$ R_i and C_i respectively represent low frequency small signal gains, equivalent resistance and capacitance associated with the input node of the i^{th} (i = 1,2,3) amplifier stage. The approximate gain A_{Oi} of the i^{th} stage amplifier is product of transconductance of driver (g_{mi}) and resistance of load R_i (Razavi, 2000) and is written as shown in Equation 5:

$$A_{Oi} = -g_{mi} * R_i \tag{5}$$

for i = 1,2,3

The equivalent resistances R_1, R_2 and R_3 are given by Equations 6a, 6b, and 6c:

$$R_1 = r_{o1} \parallel r_{o4} \parallel R_{p1} \tag{6a}$$

$$R_2 = r_{o2} \parallel r_{o5} \parallel R_{p2} \tag{6b}$$

$$R_3 = r_{03} \parallel r_{06} \parallel R_{p3} \tag{6c}$$

In Equation 6, r_{oi} represents the output resistance of the transistor M_i. The resistive load resistance of i^{th} stage (R_{pi}) (i = 1,2,3) is given by Equation 7:

$$R_{pi} = \frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_{pi}(V_{DD} - |V_{TP}|)} \tag{7}$$

The symbols used in Equation (7) have their usual meaning.
The equivalent capacitances C_1, C_2 and C_3 are given by Equations 8, 9 and 10:

$$C_1 = (1 + \frac{1}{|A_{O1}|}) * C_{gd4} + C_{gs5} + C_{gd1} + C_{db1} + (1 + |A_{O2}|) * C_{gd5} \tag{8}$$

$$C_2 = (1 + \frac{1}{|A_{O2}|}) * C_{gd5} + C_{gs6} + C_{gd2} + C_{db2} + (1 + |A_{O3}|) C_{gd6} \tag{9}$$

$$C_3 = (1 + \frac{1}{|A_{O3}|}) * C_{gd6} + C_{gsz1} + C_{gsz2} + C_{gd3} + C_{db3} + (1 + |A_Z|) * (C_{gdZ1} + C_{gdZ2}) \tag{10}$$

where C_{gdi}, C_{gdZ1}, C_{gdZ2} represent gate to drain capacitances associated with transistors M_i, M_{Z1} and M_{Z2} respectively; C_{gsi} denotes gate to source capacitances associated with transistor M_i. and A_Z is the gain of output stage inverter.

2.2. Reduction in Input Impedance

In this section analytical formulation for input impedance is developed. Figure 4a shows only one half of the feedback loop, as either Mnf or Mpf will be ON at a time. The corresponding small signal model of the gain stage is shown in Figure 4b where $Z_{in,ol}$ represent open loop input impedance and g_{mnf}, r_{onf} are transconductance and output resistance of transistor Mnf.

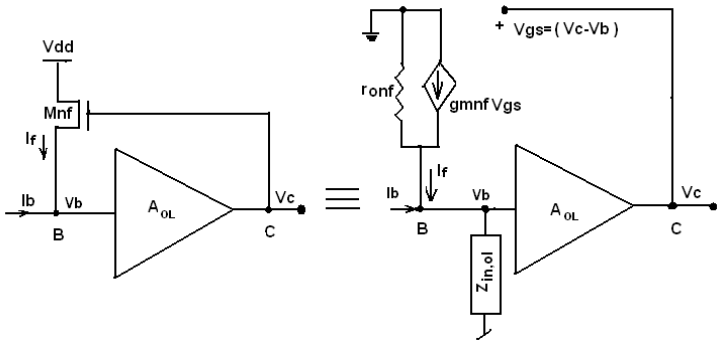


Figure 4 (a) High gain inverter stage with part of non-linear feedback; (b) its equivalent small signal model

$$V_c = [I_b + g_{mnf}(V_c - V_b)](r_{onf} \parallel Z_{in,ol}) A_{OL} \tag{11}$$

$$V_c = A_{OL} V_b \tag{12}$$

where

$$Z_{in,ol} = r_{oc} \parallel (sC_{gd4}(1 + |A_{OL}|)) \parallel sC_{gs4} \tag{13}$$

where $|A_{OL}|$ represents magnitude of open loop gain A_{OL}. Solving Equation 11 and Equation 12, the input impedance is obtained as shown in Equations 14 and 15:

$$Z_{in} = \frac{V_b}{I_b} = \frac{r_{onf} \parallel Z_{in,ol}}{1 + g_{mnf}(|A_{OL}| + 1)(r_{onf} \parallel Z_{in,ol})} \tag{14}$$

with approximation $(1+|A_{OL}|) \approx |A_{OL}|$), Equation14 reduces as follows in Equation 15:

$$Z_{in} = \frac{V_b}{I_b} = \frac{r_{onf} \parallel Z_{in,ol}}{1 + g_{mnf}(|A_{OL}|)(r_{onf} \parallel Z_{in,ol})} \tag{15}$$

Equation 15 shows that the input impedance at node B decreases due to nonlinear feedback by a factor $|A_{OL}|$ approximately.

3. SIMULATION RESULTS

The theoretical proposition is verified through simulations performed on an Orcad Pspice tool using TSMC CMOS 0.18 µm technology parameters and a supply voltage of 1.8 V. The current I_{in} was applied as input at IN1 in the form of current pulse and reference currents (I_{ref}) was input at IN2 node. The functionality of the current comparator is shown in Figures 5a, 5b and 5c for I_{ref} of 1 µA and Iin of (Iref ± ΔI) where ΔI =50 nA, 500 nA and 1000 nA, respectively. The comparator output exhibits rail-to-rail swing as the output equals the supply voltage for Iin>Iref and zero for Iin<Iref. The proposed circuit functions correctly for a minimum current difference of ± 10 nA, so the resolution is ±10 nA.

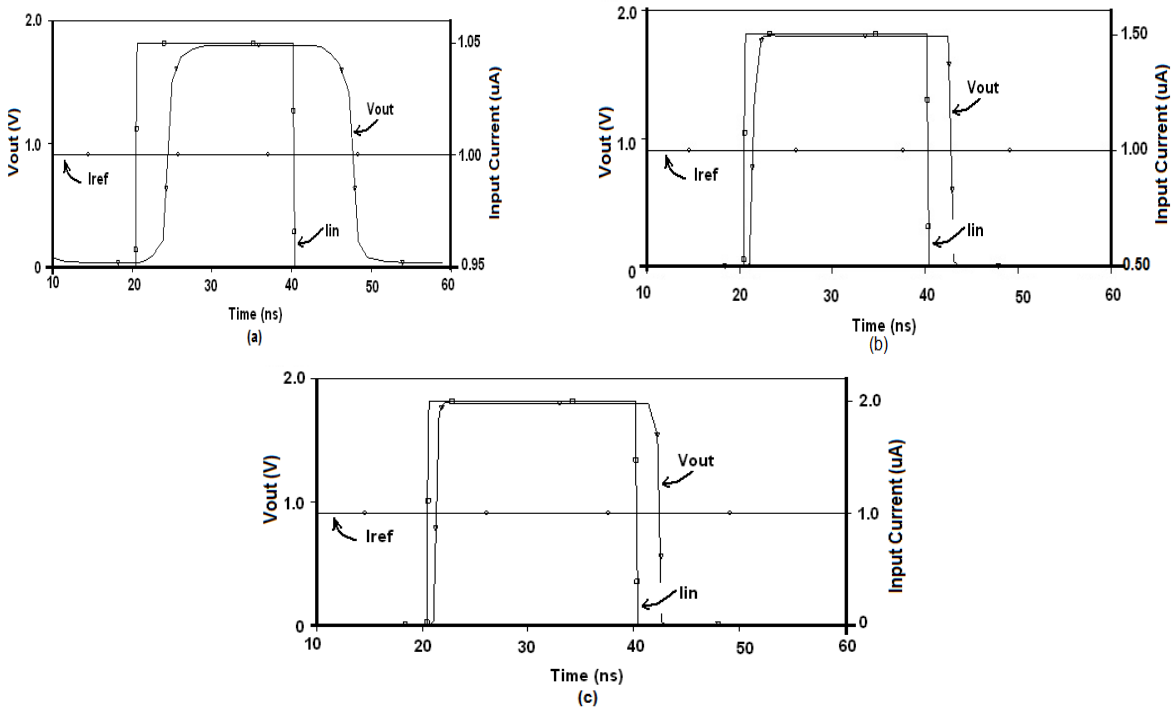


Figure 5 Comparator output for Iref of 1µA and Input current difference of: (a) ±50nA; (b) ±500nA; (c) ±1µA

The variation of performance parameters namely delay, power dissipation and Power Delay Product (PDP) with input current differences (I_{in} is varied and reference current (I_{ref}) is kept at 1 µA and is studied through a number of simulation runs. To quantify the effect of nonlinear feedback on the proposed current comparator, the structure of Figure 3 was also simulated without nonlinear feedback (i.e., Mpf - Mnf) under the same simulation conditions.

Figure 6 depicts various plots for performance parameters versus input current differences, specifically variations of input current difference with respect to delay in Figure 6a, power dissipation in Figure 6b and power delay product (PDP) in Figure 6c. Figure 6a illustrates that the propagation delay reduces with increasing current differences due to faster charging/discharging of the node capacitance. It may also be noted that there is significant improvement in the delay due to nonlinear feedback. The power dissipation remains the same

for the proposed comparator with and without feedback and the former circuit gives a better PDP. To study the effect of variation in power supply on the proposed comparator's delay, simulations were carried out at supply voltages of 1 V, 1.2 V, 1.4 V, 1.6 V and 1.8 V, respectively and various current differences. Figure 7 shows the delay as a function of both power supply and the current differences.

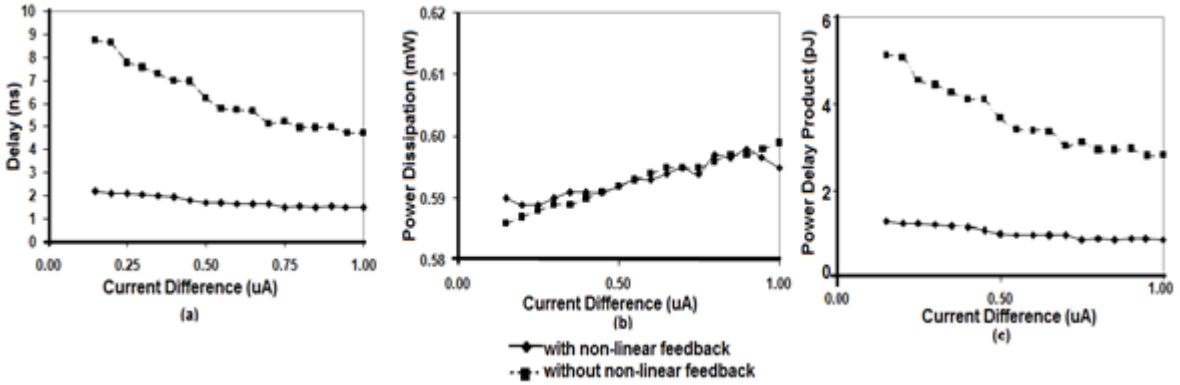


Figure 6 Variation of: (a) delay; (b) power dissipation; and (c) power delay product versus current difference

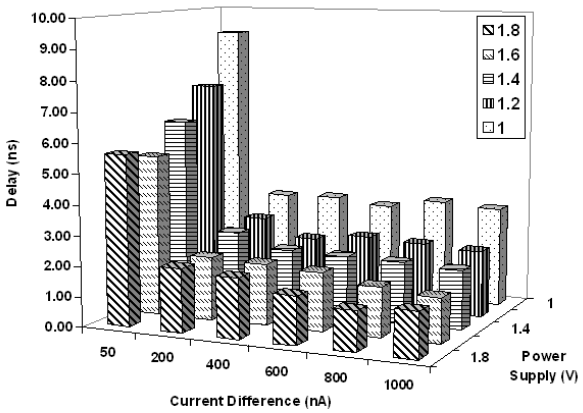


Figure 7 Delay versus variation in power supply and current difference

Process corner analysis was also carried out on the proposed comparator to study its behavior under extreme cases of process mismatch between PMOS and NMOS during manufacturing. The impact of parameter variations on the performance of the proposed comparator at different design corners is also studied and the corresponding results for delay and power dissipation are depicted in Figures 8a and 8b, respectively. In this analysis, three corners exist, namely typical, fast and slow. Slow and Fast corners exhibit carrier mobilities that are higher and lower than normal respectively. Specifically, the corner FS represents both the fast NMOS and the slow PMOS.

For the proposed current comparator, it is observed that the propagation delay is lower at the process corner FF, while the power dissipation is higher than at the process corner TT. Similarly, for process corner SS, a higher propagation delay is observed, while the power dissipation is lower than at the process corner TT.

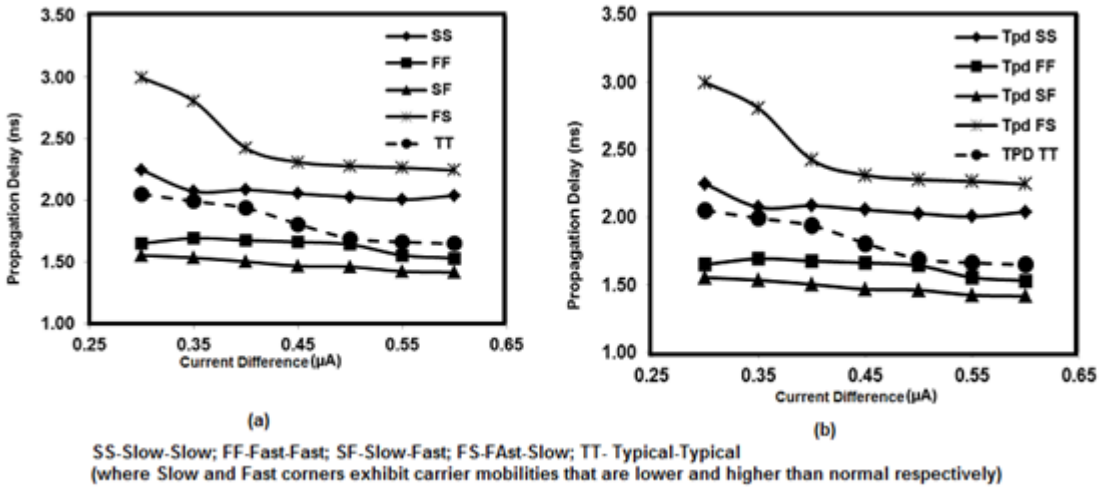


Figure 8 (a) Effect of process corner analysis on propagation delay; (b) Effect of process corner analysis on power dissipation

4. APPLICATION

In this section the proposed comparator is used to implement a 3-bit current mode flash ADC. An N bit current mode flash ADC requires 2^N-1 comparators, so seven current comparators are required for the 3-bit flash Analog-to-Digital Converter (ADC). The output of comparators is in the form of the thermometer code, so an encoder is needed to obtain desired binary output. The schematic of the 3-bit flash ADC is shown in Figure 9. The input range of the ADC is taken as 0 to 3.5 μA and seven reference currents I_{refi} (i =1 to 7) are chosen as 0.25 μA, 0.75 μA, 1.25 μA, 1.75 μA, 2.25 μA, 2.75 μA and 3.25 μA, respectively. The comparator outputs are C_7 (MSB), C_6 to C_2 and C_1 (LSB). The encoder outputs are B_2 (MSB), B_1 and B_0 (LSB), respectively.

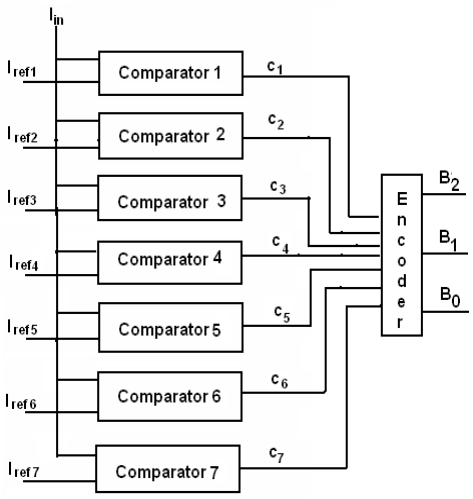


Figure 9 A 3-bit ADC

The relation between comparator and encoder output is:

$$B_0 = C_1 \oplus C_2 \oplus C_3 \oplus C_4 \oplus C_5 \oplus C_6 \oplus C_7 \quad (16)$$

$$B_1 = \overline{C_4} C_2 + C_4 C_6 \quad (17)$$

$$B_2 = C_4 \quad (18)$$

where $\overline{C_4}$ represents the complement of C_4.

The functionality of the ADC has also been demonstrated by simulations on Pspice. The ADC response is shown in Figure 10 and Figure 11 for ramp and sinusoidal inputs respectively, which confirms the correctness of the comparator behavior. The ADC transfer characteristic of Figure 9 is shown in Figure 12a along with ideal ADC. The Differential Non-Linearity (DNL) is computed to be -0.25 LSB and was plotted as in Figure 12b. It is clear that ADC does not suffer from missing codes. To compute Integral Non-Linearity (INL), the ADC characteristics are redrawn in Figure 13a with the dotted line representing the switching point where code transitions should actually take place. The INL is calculated from Figure 13a and we get maximum INL as -0.19 LSB, as plotted in Figure 13b.

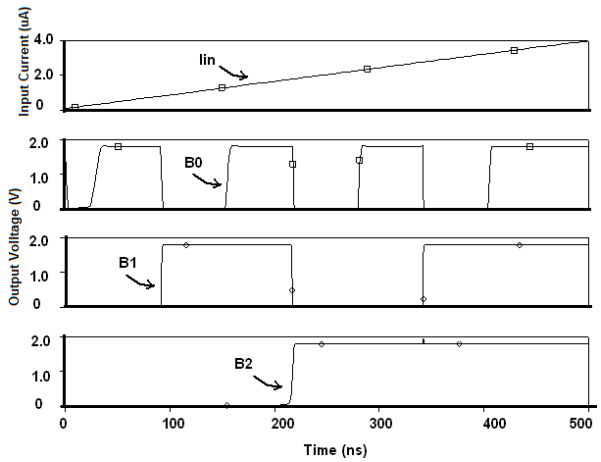


Figure 10 ADC output for ramp input

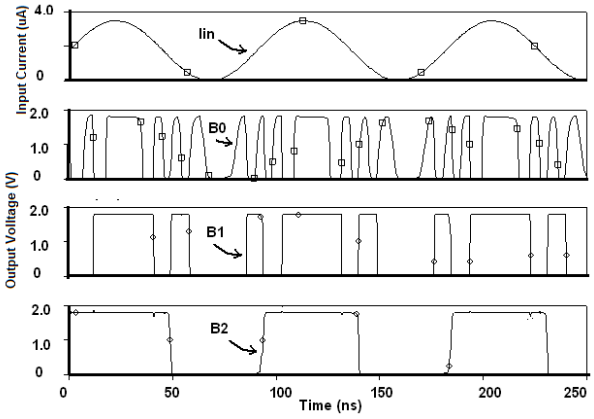
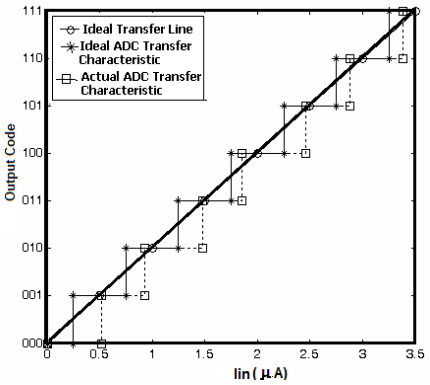
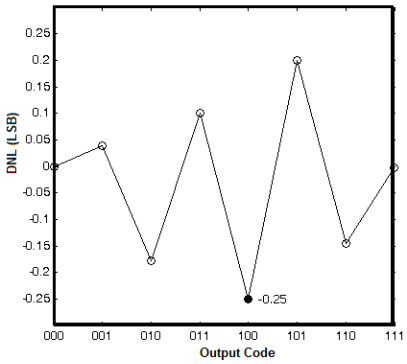


Figure 11 ADC output with sinusoidal input

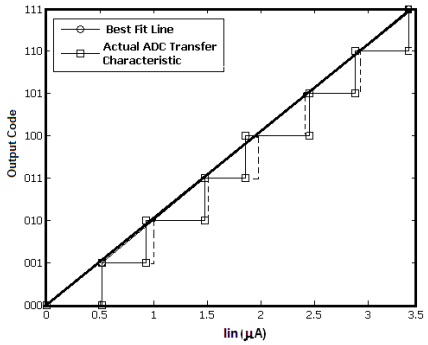


(a)

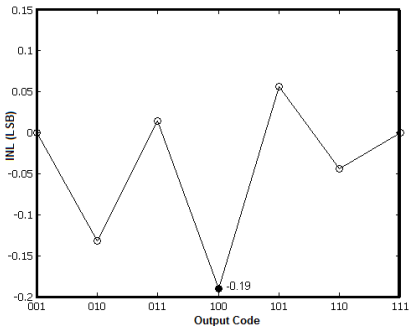


(b)

Figure 12 (a) 3-bit ADC transfer characteristic; (b) DNL versus output code



(a)



(b)

Figure 13 (a) 3-bit ADC transfer characteristic with best fit line; (b) INL versus output code

5. CONCLUSION

In this paper, new current comparator architecture is presented which utilizes nonlinear feedback around the gain stage and shown its application in a 3-bit current mode flash ADC. The analysis of the comparator around the feedback loop shows that the input impedance decreases approximately by a factor of loop gain. The proposed current mode comparator shows ±10 nA resolution and has a delay of 1.48 ns at reference current of 1 μA. The 3-bit current mode flash Analog-to-Digital Converter (ADC) shows no missing code and has Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) of -0.25 LSB and -0.19 Least Significant Bit (LSB), respectively.

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