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LINEAR I-V CHARACTERISTICS OF HIGHLY-DOPED SOI P-I-N DIODE FOR LOW TEMPERATURE MEASUREMENT

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ABSTRACT

This report is focused on the linear region of I-V characteristics of nanoscale highly-doped *p-i-n* diodes fabricated within ultrathin silicon-on-insulator (SOI) structures with an intrinsic layer length of 200 nm and 700 nm under a forward bias at a temperature range from 50 K to 250 K. The doping concentrations of Boron and Phosphorus in SOI *p-i-n* diodes are high, 1×10^{20} cm^{-3} and 2×10^{20} cm^{-3}, respectively. The linearity of I-V characteristics of the *p-i-n* diodes under a certain forward bias voltage range and temperature range from 50 K to 250 K indicate these devices are suitable for low temperature sensing purposes. We conclude that highly-doped *p-i-n* diodes produce a higher current as the temperature decreases under a certain bias voltage range. Nanoscale diodes with longer and wider intrinsic layers generate higher currents under a certain range of bias voltage and low temperature measurements.

Keywords: I-V characteristics; P-I-N diode; SOI; Sensor; Temperature

1. INTRODUCTION

According to conventional definitions, a *p-i-n* diode is similar to a *p-n* junction, but with an intrinsic layer (*i*-layer) sandwiched between the *p*-layer and the *n*-layer (Sze & Ng, 2007). In practice, however, the idealized *i*-layer is approximated by either a high-resistivity *p*-layer or a high-resistivity *n*-layer. Since the *p-i-n* diodes have found wide applications, for instance in microwave circuits or photon detection, it is important to further investigate their properties for low temperature sensing.

The high temperature fabrication process of *p-i-n* diode introduces lattice imperfections, producing deep level traps in the *i*-layer. These deep level traps act to reduce the effective lifetime and hence the stored *i*-layer charge. These traps usually dominate the overall carrier lifetime. The effective carrier lifetime (τ_{eff}) ranges in value from 1.3 ms at 200 K to 3.1 ms at 400 K, with a room temperature value of about 2 ms (Caverly, 1995).

Experimental results showed that thin-film silicon-on-insulator (SOI) *p-i-n* diodes may be suitable for temperature sensing over a wide range of temperatures (from 100 K to 400 K), reaching a high level of accuracy down to 100 K (Souza et al., 2010).

Our research group (Udhiarto et al., 2013) studied the nanosize-effect in lateral nanoscale *p-n*

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and *p-i-n* junction devices under light illumination. Current-Voltage and Current-Time characteristics were investigated at low temperatures and at room temperature for lateral nanoscale *p-n* and *p-i-n* diodes with Phosphorus (P) and Boron (B) concentrations $N_D \approx 1\times10^{18}cm^{-3}$ and $N_A \approx 1.5\times10^{18}$ cm^{-3}, respectively (as derived from secondary ion mass spectrometry).

Based on our previous research, we extend our study about *p-i-n* diodes with higher Phosphorus (P) and Boron (B) concentrations to find the importance of the *i*-layer on device characteristics under low temperature conditions. The doping concentrations of B and P in SOI *p-i-n* diodes are high, 1×10^{20} cm^{-3} and 2×10^{20} cm^{-3}, respectively. For that purpose, we design, fabricate and measure highly-doped *p-i-n* diodes with narrow and thin *i*-layer under temperatures ranging from 50 K to 250 K.

2. METHODOLOGY

2.1. Device Fabrication

We fabricated lateral nanoscale *p-i-n* diodes using a SOI structure, at the Research Institute of Electronics (RIE), Shizuoka University. The SOI structure consists of a thin Si layer on top of a 155-nm-thick buried oxide (BOX) layer and a *p*-Si substrate (doping concentration on the order of 10^{15} cm^{-3}). The devices have been designed with an *i*-layer of lengths of (*l*) 200 nm and 700 nm, respectively, and widths (*w*) of 660 nm, 680 nm, and 850 nm, respectively. However, it should be noted that the final width of the devices is significantly smaller. We used electron beam lithography (Elionix ELS 7700K) to define the fine pattern of *p-i-n* diodes. The Boron concentration (for the *p*-type region) and the Phosphorus concentration (for the *n*-type region) are both close to a 10^{20} cm^{-3} order (as measured by a four-point probe technique). This is well above the metal-to-insulator transition for Si and, therefore, the *p* and *n* regions are conductive. We also measured the silicon layer thickness to be ≈ 5 nm (by DHA-OLXS ellipsometer) at the end of all fabrication steps. The photograph of *p-i-n* diodes is shown in Figure 1 (a) and its structure is shown in Figure 1 (b).

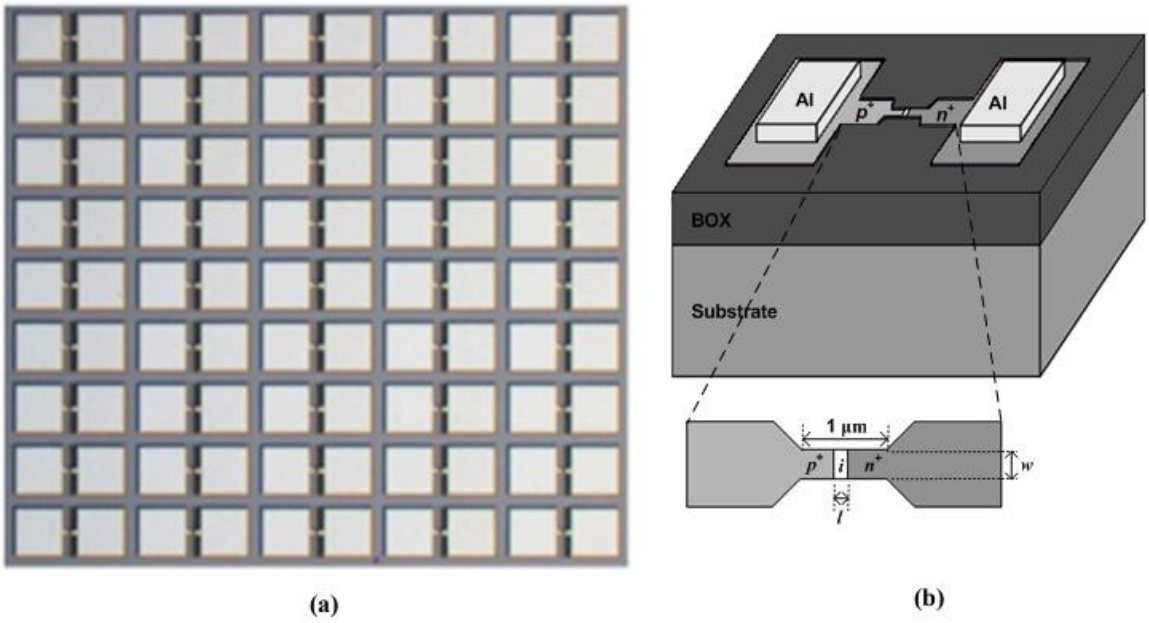

Figure 1 SOI *p-i-n* diode: a) photograph; b) structure

2.2. I-V Characteristics Measurement

We used a semiconductor precision parameter analyzer (Agilent 4156C) and a high-vacuum variable-temperature prober station to measure the I-V characteristics of a highly-doped nanoscale *p-i-n* diode. The *p*-type pad is connected to a voltage source (V_a), while the *n*-type pad and the substrate (V_{sub}) are connected to the ground. We set the temperature from 50 K to 250 K to achieve current and voltage responses in dark conditions. All of the measurements have been done in RIE.

3. RESULTS

We have investigated nanoscale *p-i-n* diodes with variations of intrinsic layer length (*l*) and width (*w*) as follows:

1) *l*=200 nm, *w*=850 nm
2) *l*=200 nm, *w*=680 nm
3) *l*=700 nm, *w*=660 nm

We measured the I-V characteristics of diode (1) and diode (2) under a forward bias voltage ranging from 1.3 V to 2.0 V and a temperature ranging from 50 K to 250 K. Meanwhile for diode (3), we measured the I-V characteristics under a forward bias voltage from 1.5 V to 2.0 V and a temperature range from 50 K to 250 K. All of the *p-i-n* diodes show a linear current response as indicated in Figures 2, 3 and 4, respectively. In this case, the diodes produce a higher current at a lower temperature.

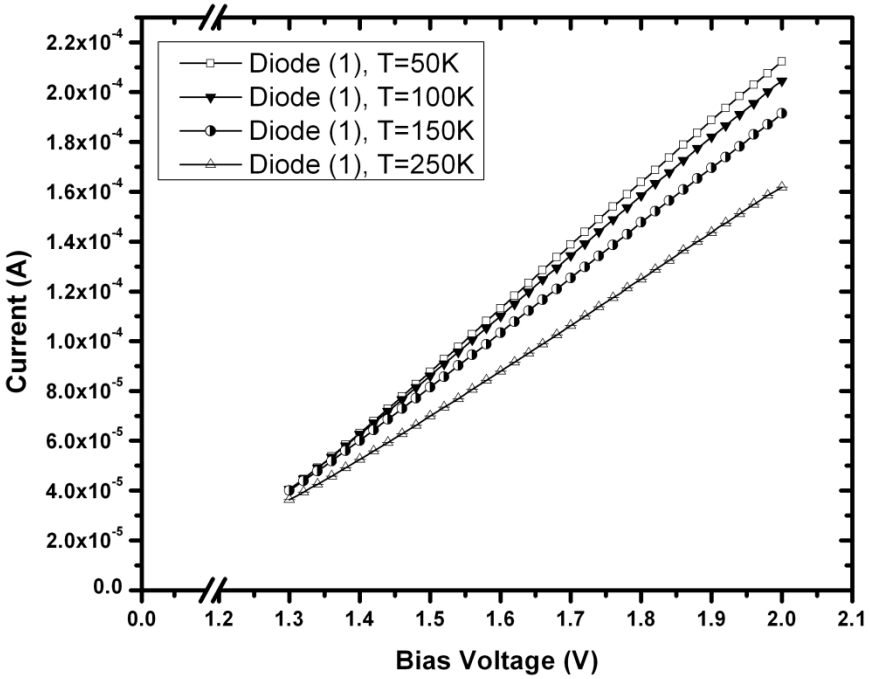

Figure 2 Linear I-V characteristics of diode (1) as a function of temperature

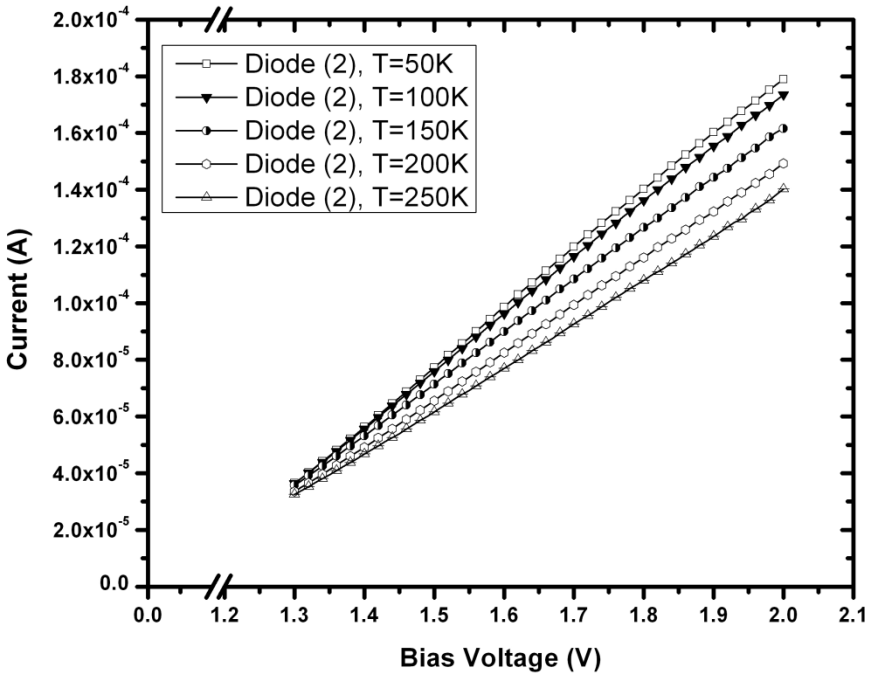

Figure 3 Linear I-V characteristics of diode (2) as a function of temperature

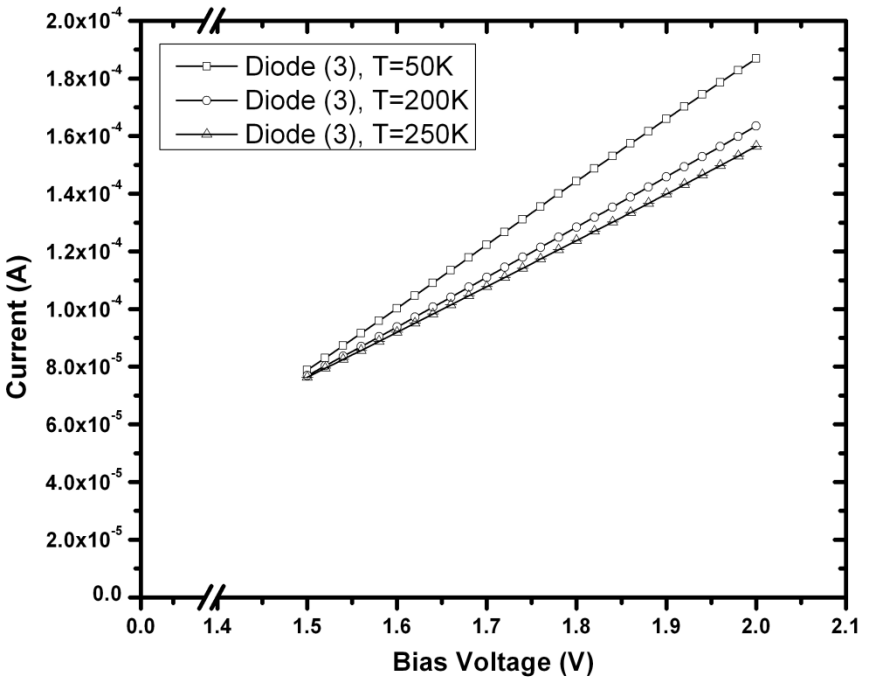

Figure 4 Linear I-V characteristics of diode (3) as a function of temperature

To show the influence of intrinsic layer width at low temperature measurement, we compared the I-V characteristics of diode (1) and diode (2) under a temperature level ranging from 50 K to 250 K, as shown in Figures 5 and 6, respectively. From these figures, we concluded that a wider intrinsic layer will produces higher current for low temperatures at a certain forward bias voltage.

For a similar purpose, to show the influence of an intrinsic layer length at a low temperature measurement, we compared the I-V characteristics of diode (2) and diode (3) under a temperature level ranging from 50 K and 250 K, as shown in Figures 7 and 8, respectively. From these figures, we conclude that longer intrinsic layers will produce a higher current at a lower temperature at a certain forward bias voltage.

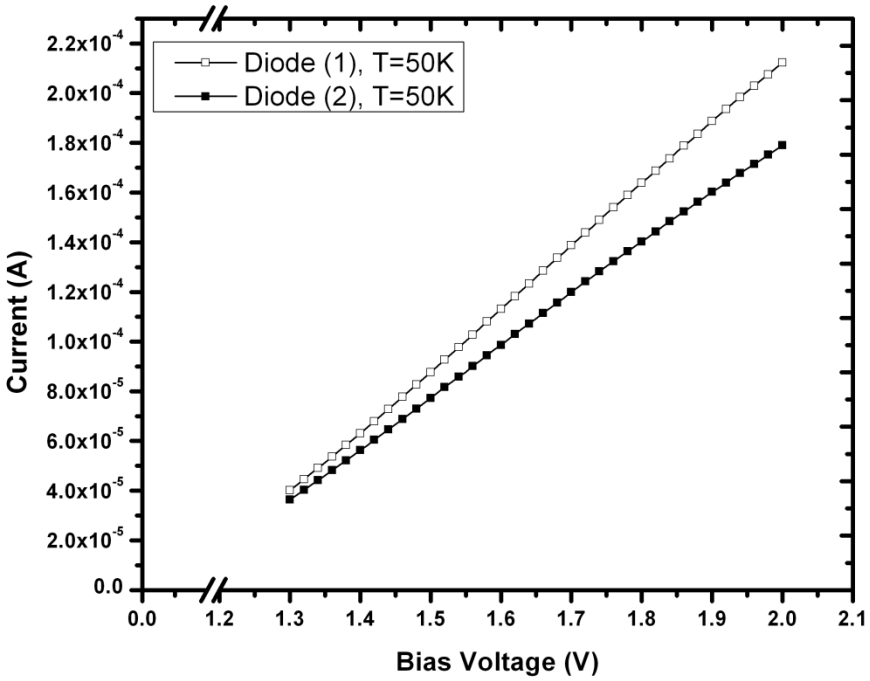

Figure 5 Linear I-V characteristics of diode (1) and diode (2) under the temperatureof50K

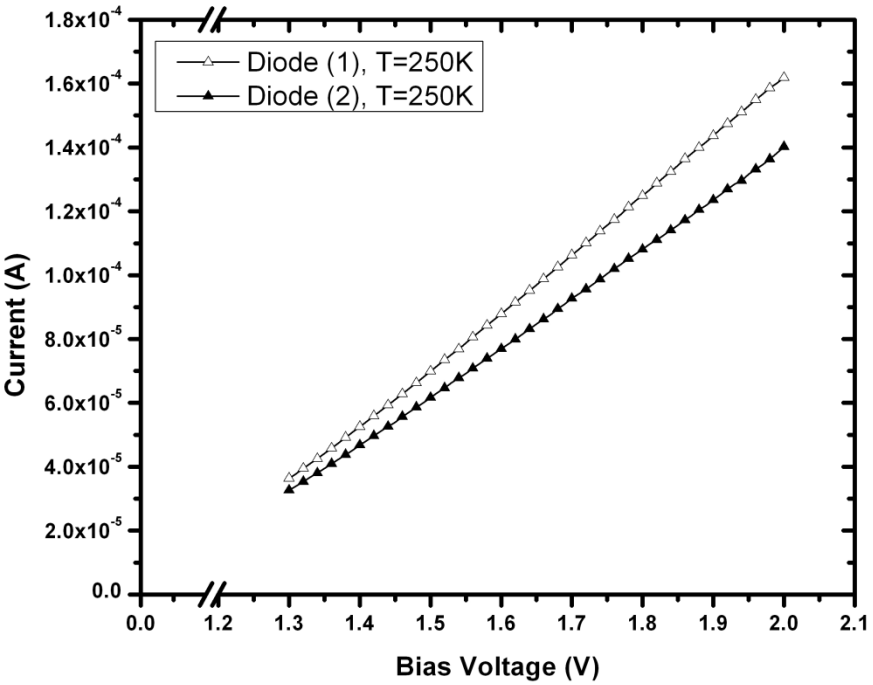

Figure 6 Linear I-V characteristics of diode (1) and diode (2) under temperature of 250 K

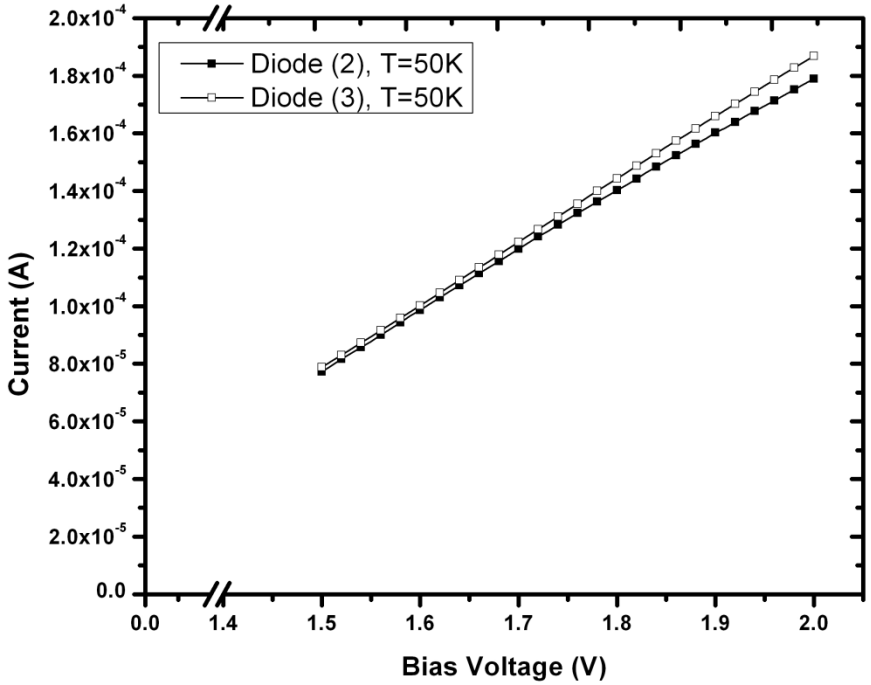

Figure 7 Linear I-V characteristics of diode (2) and diode (3) under a temperature of 50 K

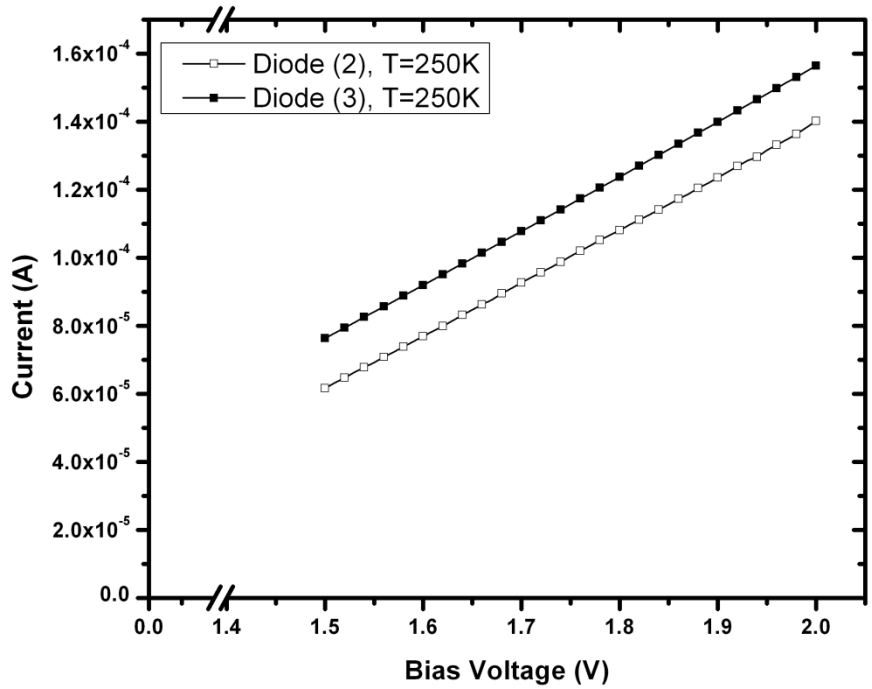

Figure 8 Linear I-V characteristics of diode (2) and diode (3) under a temperature of 250 K

4. DISCUSSION

We analyzed the linear fit of I-V characteristics under a forward bias range from 1.3 V to 2.0 V for diode (1) and diode (2), and from 1.5 V to 2.0 V for diode (3). We set the temperature range from 50 K to 250 K to achieve current and voltage responses in dark conditions. The result is shown in Table 1. The Statistics Adjusted R-Square parameter found in the range from 0.99963 to 0.99996 shows that all of the *p-i-n* diodes have linear current – voltage characteristics. The Slope Value parameter for all the *p-i-n* diodes shows that the device has a higher level of conductance at a lower temperature. For example, diode (1) has a conductance of 2.50×10^{-4} A/V at a temperature of 50 K, which is higher than a conductance of 1.82×10^{-4} A/V at a temperature of 250 K.

Under above mentioned forward bias voltage and low temperature range, where the *p*-layer has positive potential with respect to the *n*-layer, the electrons are injected from the *n*-layer and the holes are injected from the *p*-layer. The carrier density is large and varies linearly with the applied bias voltage due to the narrow depletion region and the lower barrier to carrier injection under a forward bias condition, as a result of designing the diode with high Boron and Phosphorus doping concentrations accompanied by *i*-layer length and width in the submicron range. Highly-doped *p-i-n* diode behaves like a pure resistor.

According to O'Donnel and Chen (1991), an energy band gap of Silicon is a function of temperature. The energy band gap decreases when the temperature increases. From this point of view and considering our measurement results, we proposed the energy band diagram of highly-doped *p-i-n* diode as shown in Figure 9.

Table 1 Linear fit of I-V characteristics of diode (1), (2) and (3)

Device	Temp.	Intercept Value	Intercept Standard Error	Slope Value	Slope Standard Error	Stat. Adj. R-Square
Diode (1)	50 K	-2.86×10^{-4}	5.67×10^{-7}	2.50×10^{-4}	3.41×10^{-7}	0.99987
	100 K	-2.70×10^{-4}	4.53×10^{-7}	2.38×10^{-4}	2.72×10^{-7}	0.99991
	150 K	-2.45×10^{-4}	4.66×10^{-7}	2.18×10^{-4}	2.80×10^{-7}	0.99988
	250 K	-2.02×10^{-4}	7.00×10^{-7}	1.82×10^{-4}	4.21×10^{-7}	0.99963
Diode (2)	50 K	-2.33×10^{-4}	7.23×10^{-7}	2.07×10^{-4}	4.35×10^{-7}	0.99969
	100 K	-2.21×10^{-4}	6.10×10^{-7}	1.98×10^{-4}	3.67×10^{-7}	0.99976
	150 K	-2.01×10^{-4}	3.51×10^{-7}	1.82×10^{-4}	2.11×10^{-7}	0.99991
	200 K	-1.84×10^{-4}	2.82×10^{-7}	1.66×10^{-4}	1.70×10^{-7}	0.99993
	250 K	-1.69×10^{-4}	4.29×10^{-7}	1.54×10^{-4}	2.58×10^{-7}	0.99980
Diode (3)	50 K	-2.48×10^{-4}	4.23×10^{-7}	2.18×10^{-4}	2.41×10^{-7}	0.99994
	200 K	-1.83×10^{-4}	2.55×10^{-7}	1.73×10^{-4}	1.45×10^{-7}	0.99996
	250 K	-1.64×10^{-4}	3.25×10^{-7}	1.60×10^{-4}	1.85×10^{-7}	0.99993

The effective carrier lifetime (τ_{eff}) of the *p-i-n* diode ranges in value from 1.3 ms at 200 K to 3.1 ms at 400 K (Caverly, 1995). This means the τ_{eff} value is increasing, while the temperature is rising. By substituting the τ_{eff} value into the current density equation,

$$J = (q\,\Delta n\,L)/(\tau_{eff}) \quad (1)$$

where J is the current density (A/cm^2), q is the elementary charge = 1.6×10^{-19} C, Δn is the excess electron concentration beyond equilibrium (cm^{-3}), and L is the length of intrinsic layer (cm).

the *p-i-n* diodes generate a lower current at a higher temperature as shown in Figures 2–4. The *p-i-n* diodes having a longer *i*-layer will produce a higher current density. This condition is also consistent with the linear region of the I-V characteristics of highly-doped SOI nanoscale *p-i-n* diodes, as shown in Figures 7–8

Due to fact that the τ_{eff} value is increasing, all the while the temperature is rising and a very short *i*-layer, the *p-i-n* diodes are having a wider *i*-layer, will also produce higher current density. These phenomena are shown in Figures 5–6. Therefore, highly-doped nanoscale *p-i-n* diodes using a SOI structure fabricated by a method as described in Methodology are suitable for low temperature sensing.

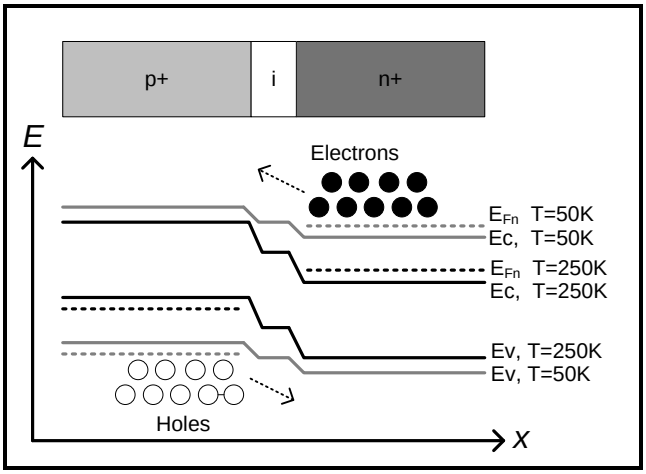

Figure 9 The energy band diagram of highly-doped nanoscale *p-i-n* diode

5. CONCLUSION

The linearity of I-V characteristics of highly-doped *p-i-n* diodes under a certain forward bias voltage range and temperature range, reading from 50 K to 250 K indicates that these devices are suitable for low temperature sensing purposes. As shown in Figures 2, 3 and 4, respectively, the *p-i-n* diodes produce higher current as the temperature decreases under a certain bias voltage range.

Diode (1) and diode (2) have the same intrinsic layer length of 200 nm and width of 850 nm and 680 nm, respectively. From data and the I-V characteristics as shown in Figure 5 and 6, we conclude that highly-doped *p-i-n* diodes with a wider intrinsic layer generate higher current under a certain range of bias voltages and low temperature measurements.

I-V characteristics measurement of diode (2) and diode (3), as drawn in Figures 7 and 8, show that highly-doped *p-i-n* diodes with a longer intrinsic layer produce higher current under certain range of bias voltage and low temperature measurement.

6. ACKNOWLEDGEMENT

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