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DESIGN AND SIMULATION OF TWO BITS SINGLE-ELECTRON LOGIC CIRCUIT USING DOUBLE QUANTUM DOT SINGLE ELECTRON TRANSISTOR

Arief Udhiarto[*1], Mohammad Ali Tamam[1], Ratno Nuryadi[2], Djoko Hartanto[1]

[1]*Electrical Engineering Department, Faculty of Engineering, Universitas Indonesia, Kampus Baru UI Depok 16424, Indonesia*
[2]*Center for Material Technology, Agency for the Assessment and Application of Technology, Puspitek Building 224, South Tangerang 15314, Indonesia*

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ABSTRACT
Electrons in a single electron transistor (SET) are transported one by one from source to drain based on the coulomb blockade mechanism. The transport rate is sensitively influenced by the presence of event a single electron charge located near the quantum dot. Based on this characteristic, we propose a Double Quantum Dot (DQD) SET to manipulate the presence of an electron in Quantum Dot (QD) as an implementation of a single-electron logic concept. The existence of an electron in the QD is used to represent logic 0 (no electron in QD) or logic 1 (an electron in QD). The logic states are sensed by a SET charge detector. Design of circuit based on DQD and SET charge detector are simulated by using SIMON 2.0 software. From the simulation, we have successfully developed a two-bit logic circuit by controlling the presence of an electron in DQD. We found that the existence of an electron in QD can be controlled by application of a gate voltage larger than 190μV. Gate should be separated from QD by a non-tunnel capacitor of 500 aF. No larger than 1 aF of interdot tunnel capacitance is required to isolate the QD from one to another. The existence of an electron in QD is successfully detected by SET based charge detector.

Keywords: Charge Detector; Double Quantum Dot (DQD); Single-Electron Logic; Single Electron Transistor (SET); Software SIMON 2.0

1. INTRODUCTION
Quantum dots are known as an artificial atom (Kastner, 1993) which offer wide variety of application. The application range from single electron transistor (Likharev, 1988; Kastner, 2000), single-photon detection (Shields, 2000; Nuryadi et al., 2006; Udhiarto et al., 2011), single electron memory (Fujiaki et al., 2008; Moraru et al., 2011) to quantum computing (Loss & DiVincenzo, 1997). In a quantum computing system, the state of logic bit is represented by a quantum bit or qubit. A theoretical study in the utilization of electron spins in a Double Quantum Dot (DQD) hydrogen molecule to realize a basic elementary gate for a quantum computer has been proposed by (Hu & Das Sarma, 2000). Another group experimentally studied the electron transport through DQD coupled in series (van der Wiel et al., 2002). They found that by changing the interdot coupling, it is possible to control the bonding type of the dots, it can be ioniclike or covalentlike bonded. In short, by arranging DQDs in series, it is possible to create an artificial molecule.

[*] Corresponding author's email: arief@ee.ui.ac.id, Tel. +6221 7270078, Fax. +6221 7270077
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The operation of Charge-qubit (Gorman et al., 2005), and charge sensing (Johnson et al., 2005; Simmons et al., 2009) in an isolated double quantum dot (IDQD) have been reported experimentally. The transfer of an electron in two distant quantum dots also has been investigated (Hermelin et al., 2013). All of those results suggest that DQD structure is a promising candidate to realize quantum logic bits. For more practical application, however, a complete design circuit with all its parameters is necessary as a guideline in the fabrication processes.

In this paper, we propose a circuit design of DQD array in series system to realize two bits single-electron logic. Two gates are utilized to control the existence of an electron in the quantum dot. The presence of the electron is sensed by single-electron transistor (SET) coupled to the quantum dot by a non-tunnel capacitance. Two bits logic circuit with all its parameters were simulated using software SIMON (Wasshuber et al., 1997).

2. EXPERIMENTAL

Schematic model of two bits single electron logic (SEL) DQD studied in the simulation is shown in Figure 1. The lower panel is a charge control consist of two metallic quantum dots connected in series by tunnel junction capacitance (C_m). The temperature is set to be 0 K in the simulation. In the following, basic operation of the circuit is described. Source and drain are used to supply and to pass an electron from QDs. Each QDs is connected to a gate via non-tunnel capacitance, Cg1 and Cg2 of 500 aF. Gates are used to control the dot potential. Applying positive gate voltage will reduce the QD potential and hence allowing an electron to tunnel to the dot. Lowering the gate voltage will increase the dot potential and eventually remove the electron from the dot. Two charge detectors in the upper panel are used to sense the states of the dots. The charge detectors are connected to the dots through non-tunnel capacitance. Source-drain bias (V_{ds}) is kept constant at 20 μV. Tunnel junction resistance (R_L, R_m, R_R) and tunnel junction capacitance (C_L, C_R) are set to be 30 kΩ and 10^{-18} F respectively. Parameters used in the simulation have been chosen based on theory and typical values obtained from experimental results. Gate capacitances (C_{g1}, C_{g2}), gate voltages (V_{g1}, V_{g2}), and coupling capacitance C_m are parameter to be defined from the simulation results.

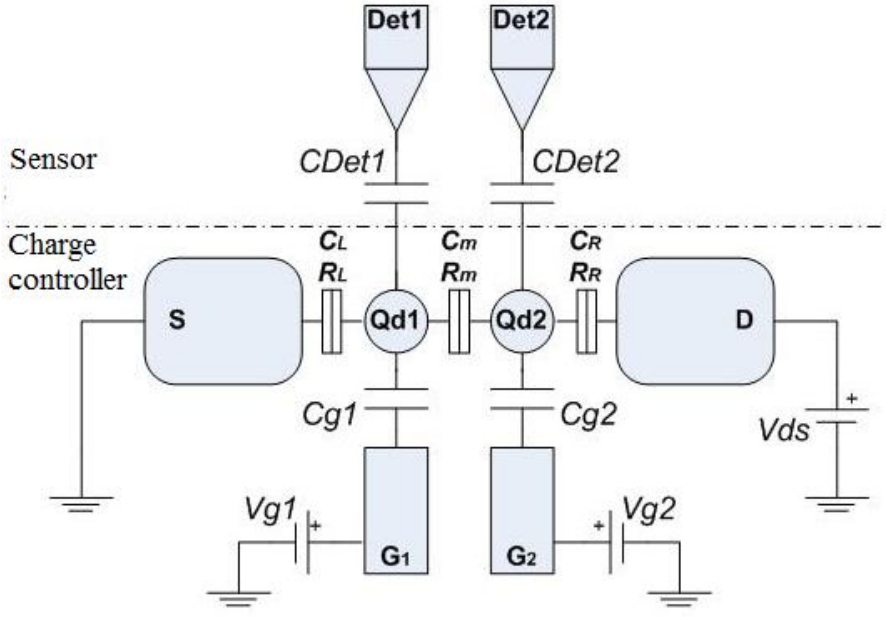

Figure 1 Schematic DQDs with two control gates

3. RESULTS AND VALIDATION

We swept gates voltage from 0 V to 1 mV. Figure 2 shows that by increasing the gate voltage an electron is sequentially injected into the dots one by one. Left and right vertical axes are charge in QD_1 and QD_2 respectively, while horizontal axis is the applied gates voltage.

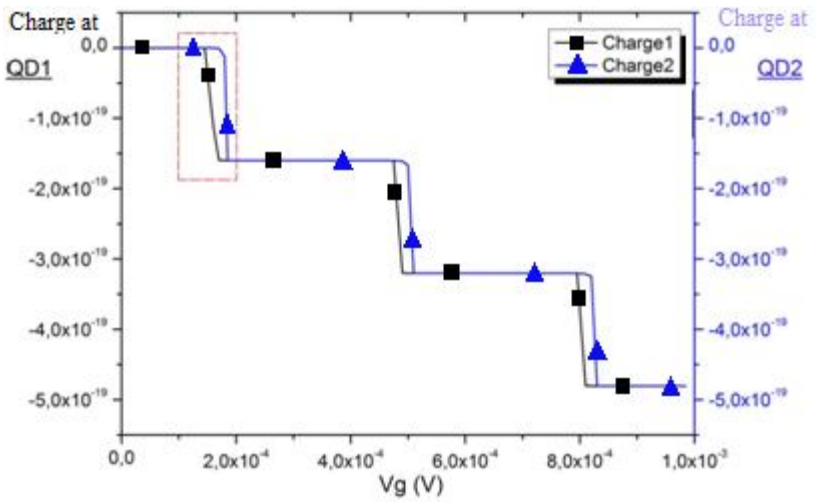

Figure 2 Number of injected electrons in the QDs versus applied gate bias

Number of injected electron in QD1 and QD2 increases discretely by increasing gate voltage. The existence of the first electron in the dot is clarified by the charge value which is equal to -1.6×10^{-19} and is reached when gate voltage is around 150 μV as indicated by red square. The second and the third electrons are injected to the dot when gate voltage is around 500 μV and 800 μV respectively.

As indicated by the red square mark, the minimum gate voltage required to inject the first electron in QD is around 150 μV to 200 μV. A square pulse is used as an input logic and is used to evaluate if the circuit can produce the correct output. By setting a square pulse with the amplitude in the range of 150 μV to 200 μV, we systematically simulate the output signal as function of the applied gate voltage. As shown in Figure 3, the output signals in both QDs are perfectly reproduce the input signal (upper panel) when the applied gate voltages are larger than 190 μV. The charging and discharging mechanism of the QDs are illustrated in Figure 4.

Figure 4 (a) is schematic two bits SEL DQDs circuit. Figure 4 (b)-(f) are the corresponding QDs potential and the electrons position for different applied gate voltages (Vg1 and Vg2). Figure 4(b) illustrates the QDs potential when both Vg1 and Vg2 are 0V. Since both QDs potential are above source-drain Fermi energy, no electrons are able to tunnel to the QDs and hence both QDs are empty. By applying Vg1 = 190μV and keep Vg2 = 0 V, the potential in Qd1 is reduced allowing an electron to tunnel from the source to QD1 as shown in Figure 4(c). This situation corresponds to (1.0) state. By changing Vg2 to 190 μV and Vg1 to 0V the opposite situation occurs, the potential in the QD2 is now below the potential of QD1, as a result electron in QD1 tunnels to QD2 (Figure 4 (d)). This state corresponds to (0.1) logic. By applying Vg1 = 190 μV, another electron tunnels from source to QD1 as shown in Figure 4 (e). This is (1.1) logic state. Logic (0.0) state is obtained by resetting the gate voltage (Vg1 and Vg2) to 0 V (Figure 4 (f)). Based on this mechanism, two bits electron logic based DQDs can be realized.

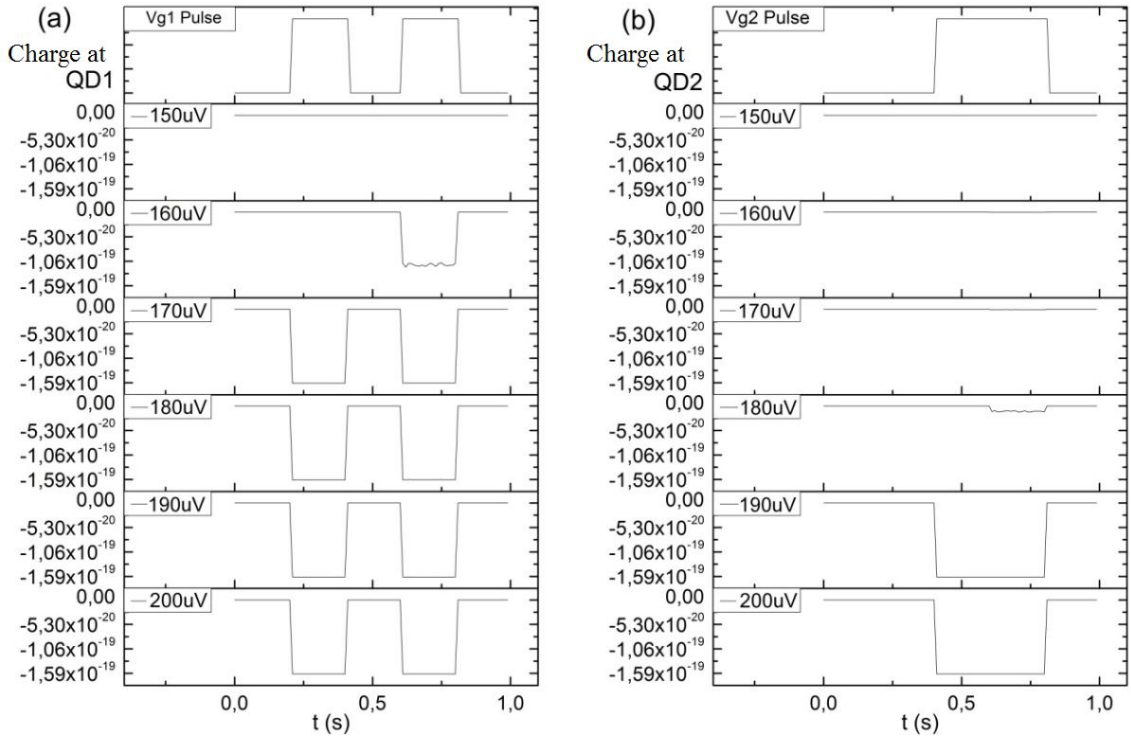

Figure 3 Charge in the QD (a) 1 and (b) 2 for different applied pulse amplitude, increasing from top. The upper panel is the applied pulse. The minimum gate voltage to produce the correct signal is 190 uV

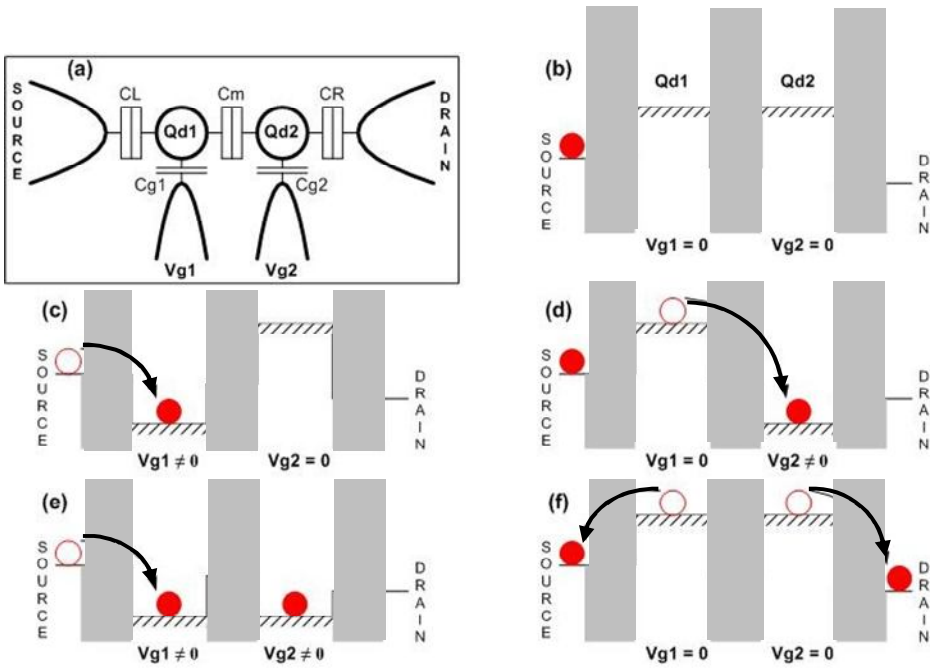

Figure 4 Schematic circuit of DQD (a) and its corresponding potential as function of applied gate voltages (b) – (f)

Next, we simulate the effect of interdot capacitance (C_m) in order to obtain the appropriate capacitance. We systematically increase C_m from 1 aF to 100 aF. As shown in Figure 5, for C_m = 100 aF, the state of one QD will be strongly affected by the state of another QD. As a result, the detected charge in the dots is not anymore agreed with the applied gate pulse. This is caused

by a strong coupling between dots that make QDs behave like two atoms in a molecule. We found that C_m should be 1aF or lower in order to isolate the dot one from the other.

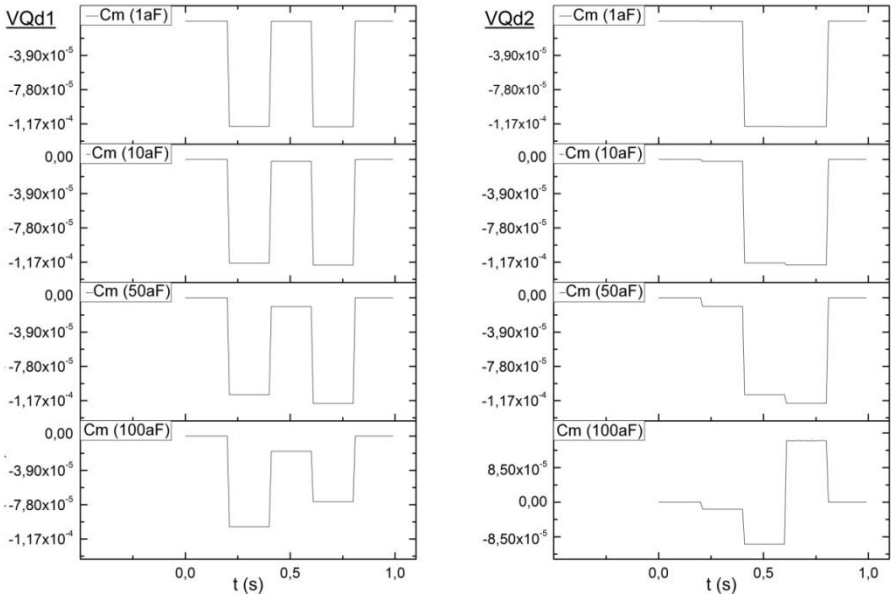

Figure 5 Charge of QD1 and QD2 for several interdot capacitance (C_m). By increasing C_m, charge in a QD will gradually affect another QD. C_m = 1aF or lower is required to isolate QD1 from QD2

Using the obtained parameters (Vg = 190 μV and C_m = 1 aF), we simulate the potential and the charge of QDs when an input signal is applied in the gate as shown in Figure 6. It can be seen that the potentials (middle panel) and charges (lower panel) in both QDs are in a good agreement with the applied pulse for each gate (upper panel). The opposite polarity between applied voltage and the QD potential comes from the fact that applying positive voltage is equal to reducing the potential. Negative polarity with a value of 1.6×10^{-19} C in the charge meter (lower panel) indicates that exactly an electron is stored in a QD.

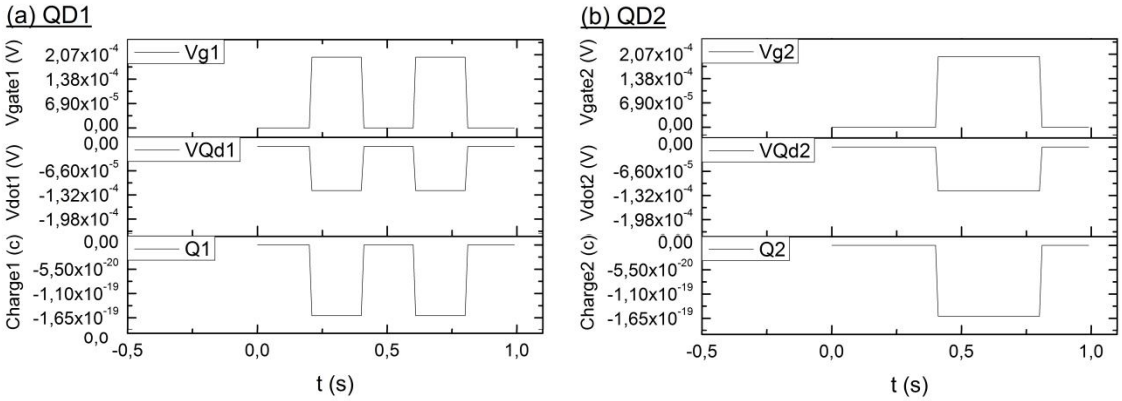

Figure 6 The potential and charge states as function of applied gate input for (a) QD1 and (b) QD2. The QDs potential and charge are in a good agreement with the applied gate input

So far, the output of the QD charges is measured by a charge meter provided by the software. For more realistic application, we replace the charge meter with a SET based charge detector as shown in Figure 7. The SET based charge detector consists of a tunnel junction in the source (*CsDet1*, *CsDet2*), tunnel junction in the drain (*CdDet1*, *CdDet2*), and gate capacitance

(*CgDet1, CgDet2*). All of the capacitances and resistances of the tunnel junction are set to be 1 aF and 30 kΩ respectively. 500 aF of gate capacitances are connected to the gate voltage source. The charge detectors are coupled to QDs via 50 aF of detector capacitances (*CDet1, CDet2*). The current (Idet1, Idet2) flowing in each SET are measured in order to monitor the QDs states.

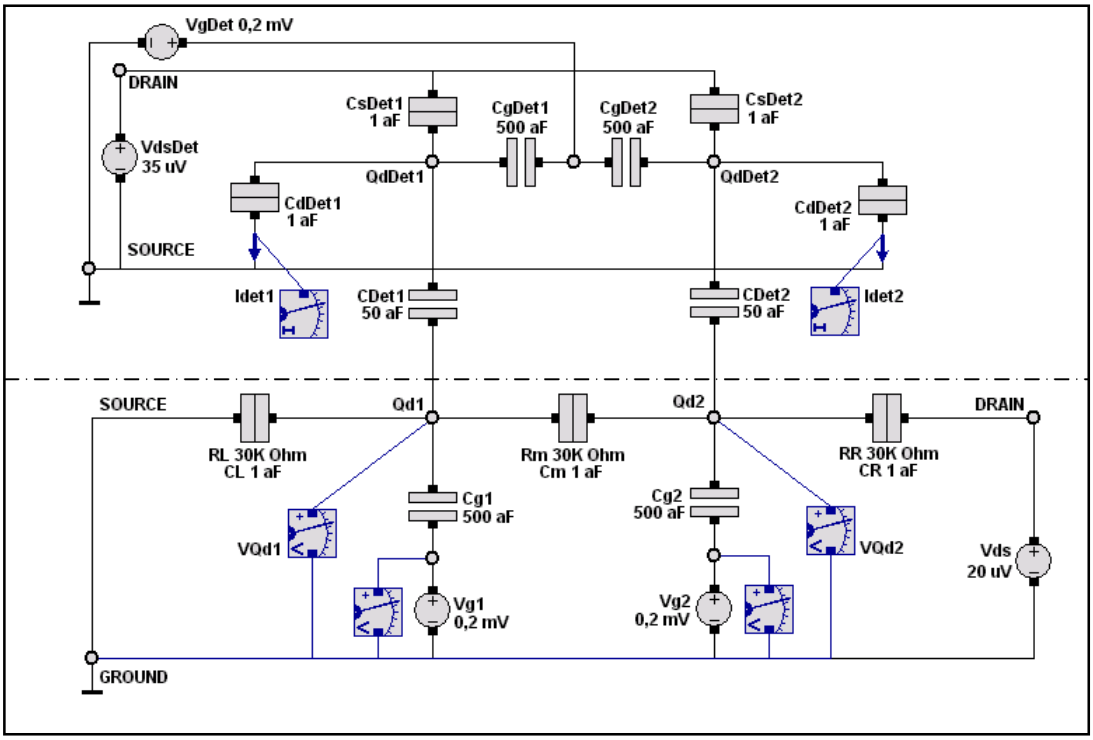

Figure 7 DQD with SET charge detector circuit

Figure 8 shows the simulation results. We found that the measured currents in the charge detectors are in a good agreement with the applied gate input, although a noise feature is observed on top of the signal. These results suggest that the propose DQD circuit with appropriate parameters can be used to realize two-bit single-electron logic.

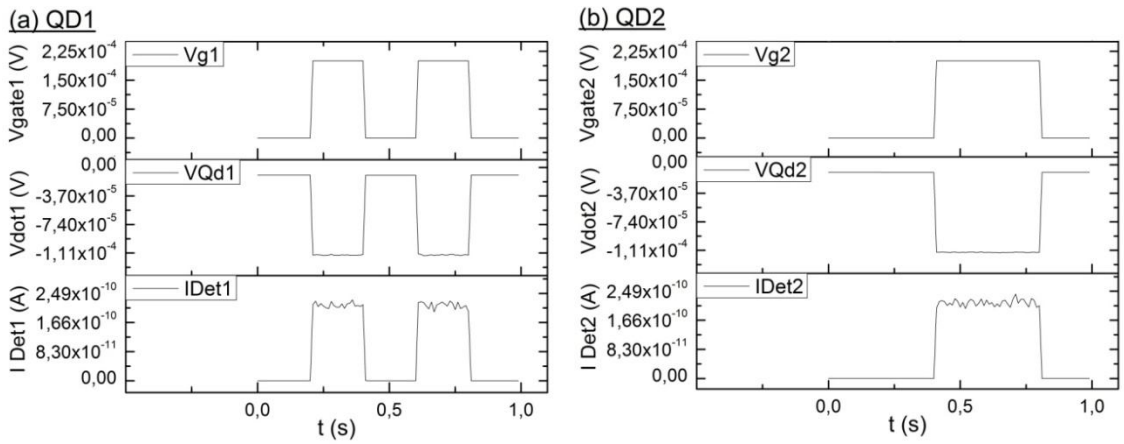

Figure 8 Measured current in the SET charge detector (lower panel) versus applied gate input (upper panel) for (a) QD1 and (b) QD2. The measured current successfully follows the input signal

4. CONCLUSION

We have successfully developed two bits single-electron logic circuit using Double Quantum Dot (DQD) array in series. The output logic is in a good agreement with the input logic as far as the minimum gate voltage and the maximum interdot capacitance are not less than 190 μV and not higher than 1 aF respectively. The results may give an insight to realize quantum dot based quantum computing system.

5. ACKNOWLEDGEMENT

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