International Journal of Technology (2011) 2: 156-163
ISSN 2086-9614

DESIGN OF CMOS RFIC UWB CARRIER-LESS AND CARRIER-BASED TRANSMITTERS

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(Received: May 2011 / Revised: June 2011 / Accepted: June 2011)

ABSTRACT

This paper presents new carrier-based and carrier-less ultra-wideband (UWB) transmitter architectures and their CMOS implementation. The carrier-based transmitter designed using a 0.18-μm CMOS process adopts a double-stage switching to enhance RF-power efficiency, reduce dc-power consumption and circuit complexity, and increase switching speed and isolation. Measurement results show that the generated UWB signal can vary from 2 V peak-to-peak with 3-dB 4-ns pulse width to 1 V with 0.5 ns, covering 10-dB signal bandwidths from 0.5 to 4 GHz, respectively. The generated UWB signal can be tuned to cover the entire UWB frequency range of 3.1 to 10.6 GHz. The carrier-less transmitter integrates tuning delay circuit, square-wave generator, impulse-forming circuit, and pulse-shaping circuit in a single chip using a standard low-cost 0.25-μm CMOS process. It can generate monocycle pulse and Gaussian-type impulse (without the pulse-shaping circuitry) signals with tunable pulse duration. Measured results show that the carrier-less transmitter can produce 0.3–0.6 V peak-to-peak monocycle pulse with 140–350 ps tunable pulse-duration and 0.5–1.3 V peak-to-peak impulse signal with 100–300 ps tunable pulse-duration.

Keywords: CMOS RFIC; transmitter; UWB transmitter; UWB system; UWB communications and radar

1. INTRODUCTION

Ultra-wideband (UWB) technology has received significant interests, particularly after the FCC's Notice of Inquiry (FCC Gov, 1998), and Report and Order (FCC Gov, 2002) or unlicensed uses of UWB devices within the 3.1–10.6 GHz frequency band. UWB techniques are promising technology, capable of both accurate position location and high-rate, short-range ad-hoc networking as well as high-resolution sensing.

Carrier-based UWB signals have been widely used in various radar and communication applications (Fontana, 2004). They hold the advantage of more convenient spectrum management and less distortion through antennas (Fontana & Larrick, 2000). In typical UWB transmitters, the generated carrier-based UWB voltage signal needs to be sent to a wideband power amplifier (PA) to achieve the required power level. This approach suffers from two major disadvantages: the design challenges of a UWB PA and low power efficiency in low pulse repetition frequency (PRF) situation.

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Carrier-less UWB communication and radar systems use ultra-short duration pulses in the sub-nanosecond regime, instead of the more conventional continuous sinusoidal waves, to transmit information. The pulse directly generates a very wide-band instantaneous signal with various duty cycles depending on specific usages. A carrier-less UWB system coherently and directly converts the received radio frequency (RF) pulse-train signal into a baseband digital or analog output signal in one stage. No intermediate frequency stage is needed, thus greatly reducing the system complexity. Carrier-less UWB technique is attractive for high-data-rate, short-range communication, radar and sensor systems. The pulse generator and antenna are two key components in both the transmitter and receiver in UWB carrier-less systems. Monocycle pulse has band-limited characteristics without DC component, facilitating its transmission through practical antenna, and is normally preferred. Meanwhile, pulse with tunable duration has both advantages of increased penetration or range and fine range resolution and is attractive for UWB systems (Han & Nguyen, 2006). The transmitted and received signals of UWB systems require antennas not only radiating energy efficiently but also having linear phase response.

In this paper, we present new carrier-based and carrier-less UWB transmitters designed using CMOS RFIC process. The CMOS carrier-based transmitter module covers the entire 3.1-10.6 GHz UWB band with variable bandwidth of 500 MHz to 4 GHz. It is not only power-efficient but also reduces power consumption, enhances switching speed and isolation, and reduces circuit complexity The CMOS carrier-less transmitter is capable of both tunable monocycle pulse (140-350 ps) and impulses (100-300 ps).

2. CARRIER-BASED UWB TRANSMITTER

Figure 1 shows the block diagram of the carrier-based UWB transmitter, consisting of a Voltage-Control Oscillator (VCO), a buffer, a SPST switch, and two pulse generators. In this approach, power switching is used to perform the signal multiplication, instead of mixing as used in the more typical UWB transmitter structure. The transmitter's principle is based upon the concept of generating a carrier-based UWB signal by gating a single-tone signal with a small time window, thereby only producing signal during a small time period. A double-stage switching procedure, using two pulse generators of wide and narrow pulses, and two switches, is adopted in the proposed transmitter to remedy the switching speed limitation of the buffer, inherent in CMOS circuits, to achieve sub-nanosecond gating required in UWB signal generation.

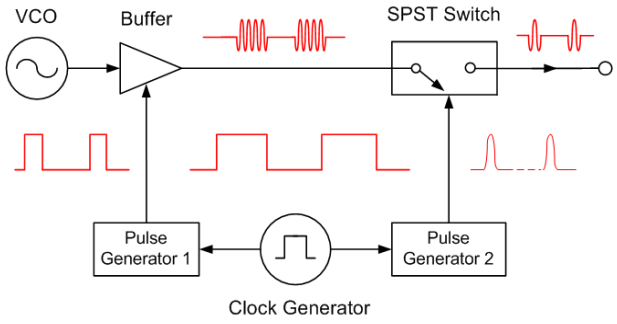


Figure 1 Carrier-based UWB transmitter

The VCO generates carrier signals that define the center frequencies of UWB signal to feed the buffer to realize sufficient transmitted power and proper output impedance matching. The buffer is gated through its internal switch (first-stage switching) using a wide pulse produced by the pulse generator 1, which should be wide enough to allow the buffer to start and reach stabilization. The second-stage switching, performed by the SPST switch and pulse generator 2 generating narrower pulses, is then used to reduce the pulse width of the generated signal,

making it an UWB signal having spectrum bandwidth of at least 500 MHz as defined by FCC (FCC Gov, 1998). Pulse generators 1 and 2 are synchronized using a common clock generator as shown in Figure 1.

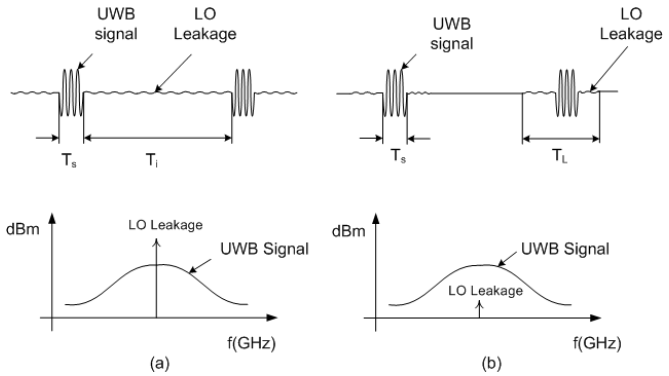


Figure 2 Effects of power leakage using (a) single-stage and (b) double-stage switching

Figure 2 shows the effects of power leakage and demonstrates the need for two switching stages. In Figure 2(a), only the second-stage switching is used. T_s stands for the pulse width of the UWB signal, while T_i is the interval between two consecutive pulses. During the time the second-stage switching is off, the LO signal (i.e., the VCO's signal) still manages to arrive at the transmit antenna due to limited SPST switch isolation. Although this LO leakage has much smaller amplitude than the transmitted UWB signal, it can still accumulate sufficiently large power over the duration T_i to over-drive the UWB signal on the transmitted spectrum. When this happens, a high-power single tone would be observed at the carrier frequency above the UWB signal spectrum. To avoid this problem, the signal-to-leakage ratio should be much higher than T_i / T_s. For instance, for a 1-ns UWB signal pulse to be transmitted at 10-KHz PRF with negligible power leakage, the ratio T_i / T_s is roughly about 10^5 and an isolation of much more than 50 dB is thus required to satisfy the leakage requirement if only one switching stage was used (i.e, the second stage).

This level of isolation is difficult to achieve in conventional CMOS switches. In Figure 2(b), both switching stages are applied. The LO leakage only appears during the time the buffer is on; i.e., within the time widow T_L, which is usually no longer than 10 ns. The isolation of the second-stage switching is only required to be larger than T_L / T_s. In this case, 30-dB isolation is sufficient to ensure small LO leakage regardless of the PRF used. For CMOS switching, 30-dB isolation is a modest requirement and can be achieved by careful design.

The carrier-based UWB transmitter covering the entire UWB band of 3.1-10.6 GHz was realized using a pulse generator-SPST switch CMOS chip, designed and fabricated using the TSMC 0.18-μm CMOS process, and an external frequency synthesizer. It was implemented without the pulse generator 1 and the VCO and buffer replaced with an external frequency synthesizer. The CMOS chip's microphotograph is displayed in Figure 3. The die area of the whole circuit is 850 μm by 700 μm including input and output on-wafer pads. The measurement was conducted on-wafer. The frequency synthesizer supplied the LO signal feeding the input port of the pulse generator-SPST switch chip. A 15-MHz clock was used to drive the on-chip pulse generator. The whole circuit consumes less than 1-mA DC current.

Figure 4 displays the time-domain waveform and the spectrum of a measured UWB signal. The UWB signal has a 3-dB pulse width of 4 ns and a 10-dB bandwidth of 500-MHz at 5-GHz center frequency, which conforms to the FCC's minimum UWB bandwidth requirement. The UWB signal amplitude is 2-V (peak-to-peak) and its amplitude at 5 GHz is -20 dBm. The 2-V

peak-to-peak voltage is the maximum voltage level corresponding to the SPST being turned on completely. The side-lobe level is below –15 dBc. By increasing the external biasing voltage for the pulse generator, the pulse width of the UWB signal is reduced. When the pulse width is reduced to a certain value, the amplitude of the UWB signal, however, diminishes due to the fact that the SPST switch cannot be completely turned on any more, which results in partial reflections of the carrier signal. When the amplitude of the UWB signal decreases to half of its maximum value (2V), the corresponding duration is defined as the minimum pulse width. This minimum pulse width is measured as 0.5 ns.

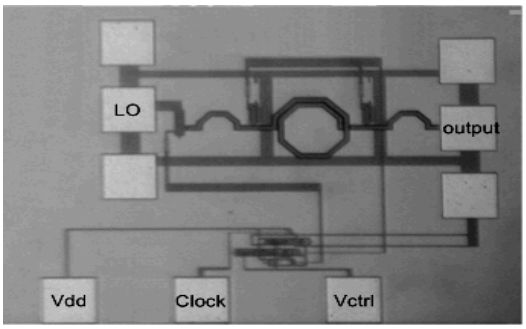


Figure 3 Microphotograph of the 0.18-µm CMOS chip integrating the pulse generator and the SPST switch

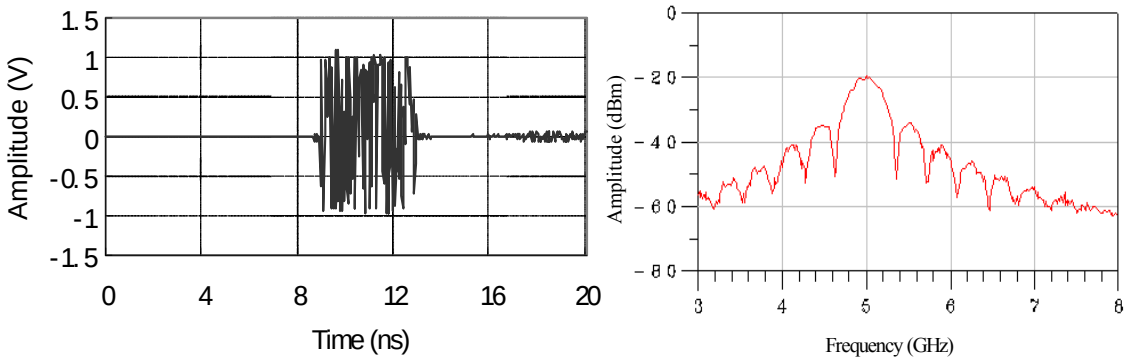
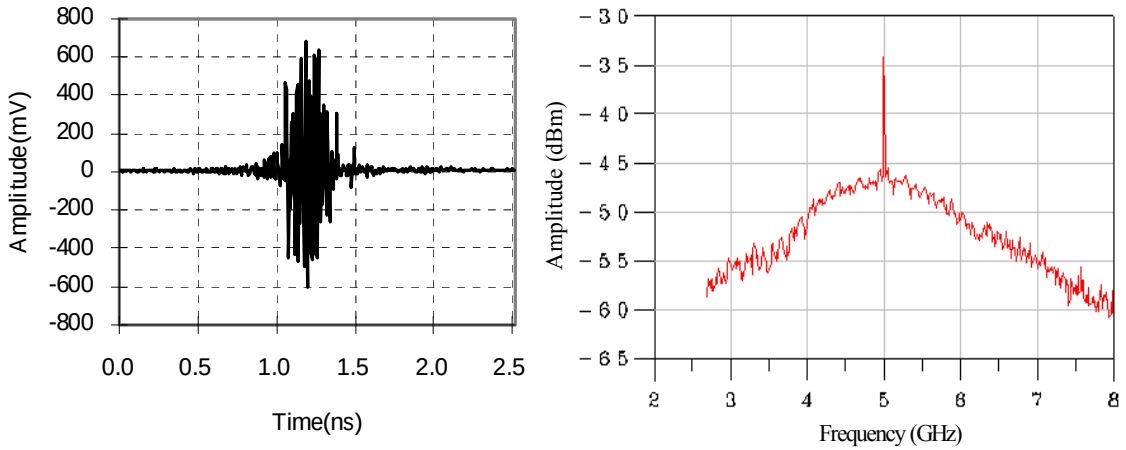


Figure 4 Measured UWB signal having 500-MHz bandwidth: (a) time-domain waveform, and (b) spectrum

Figure 5 displays the UWB signal with this minimum pulse width. The peak-to-peak voltage amplitude is around 1V. The 10-dB bandwidth is around 4 GHz. The LO leakage overshooting can be clearly seen from the spectrum of this signal because only a single-stage switching is used here. This LO leakage confirms experimentally the need of a double-stage switching for the carrier-based UWB transmitters (Figure 1) as explained earlier. With another stage of switching, the LO leakage can be reduced to a negligible level. With both levels of switching, the efficiency of the transmitter will be reduced due to the added power consumptions of the VCO and buffer, with the latter particularly dominating the efficiency owing to its larger power consumption. It is, however, relatively easy to achieve high power efficiency for a single-tone buffer. The pulse width of the obtained UWB signal can be further reduced by increasing the bias voltage of the pulse generator, hence achieving wider signal bandwidth than 4 GHz. This, however, is obtained at the expense of its signal amplitude.

Figure 6 shows the measured spectrums of different UWB signals, obtained by varying the carrier frequency at a certain bias voltage for the pulse generator, demonstrating that the entire UWB band of 3.1-10.6 GHz can be achieved with the developed CMOS chip by using a multi-band signal source.



(a) (b)

Figure 5 Measured UWB signal having 4-GHz bandwidth: (a) time-domain waveform, and (b) spectrum

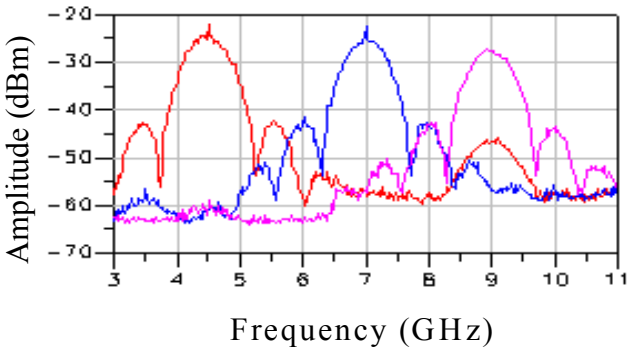
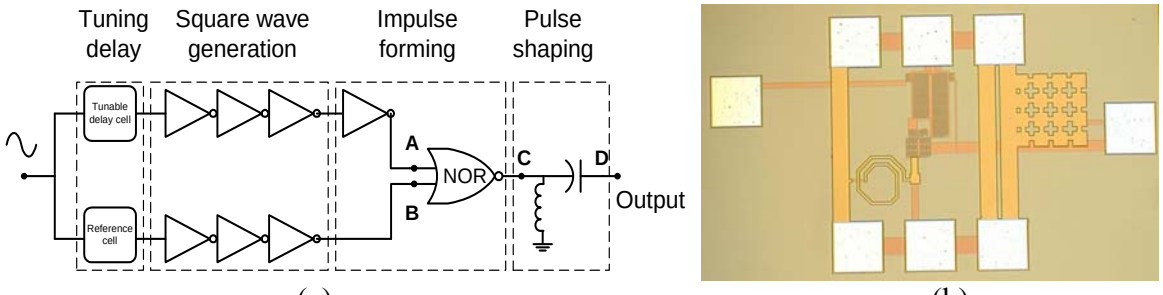


Figure 6 Measured spectrums of UWB signals covering the 3.1-10.6GHz UWB band

3. CARRIER-LESS UWB TRANSMITTER

The carrier-less UWB transmitter is based on tunable pulse generator. Figure 7 shows the CMOS tunable monocycle pulse generator chip. It integrates a tuning delay circuit, a square-wave generator, an impulse-forming circuit, and a pulse-shaping circuit in a single chip. The chip was fabricated using the standard, low-cost TSMC 0.25-µm CMOS process.



(a) (b)

Figure 7 Schematic (a) and photograph (b) of the CMOS UWB tunable monocycle pulse generator

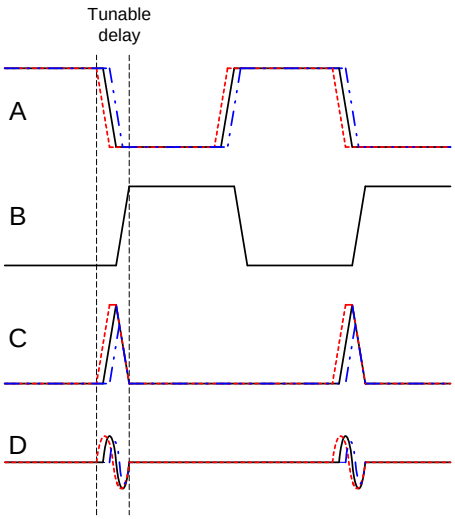


Figure 8 Illustration of signal shapes at each node of the tunable monocycle pulse generator shown in Figure 7

Figure 8 illustrates the voltage variations at different nodes *A, B, C,* and *D* of the tunable monocycle pulse generator designated in Figure 7 when a 10-MHz sinusoidal clock signal is fed to the generator. As shown in Figure 7, the input clock signal is divided equally into two paths: one signal passing through the tunable delay cell in the top path and another going through the reference cell in the bottom path. At node *B*, a square-wave signal (0V to V_{dd}) with very short rising and falling times is generated and functions as one of the inputs to the following NOR gate block. By choosing a suitable control voltage V_{ctrl} for the tunable delay cell between 0V and V_{dd} , another square wave with a different delay time is generated at node *A*. This signal is the reversed replica of that at node *B* with a certain time difference and acts as another input signal to the NOR gate block.

The output of the NOR gate block is at high state (V_{dd}) only when the inputs to the NOR gate are both at low state (0V). For all the other input states, the output are always low (0V). When these two reversed square waves at *A* and *B* are fed to the NOR gate block, a narrow impulse-like signal is generated at node *C*. The width of this impulse signal depends on the relative time-delay between these two square-wave signals and their rising and falling edges. The impulse signal at node *C*, therefore, can be easily generated with a continuously tuning duration. A smaller delay time between nodes *A* and *B* generates a narrower impulse with a smaller peak-to-peak voltage on node *C*, while a larger delay time produces a broader impulse with a higher peak-to-peak voltage. When the tunable impulse signal is sent to the pulse-shaping circuit, a monocycle pulse signal with different durations is achieved at node *D*.

The CMOS tunable monocycle pulse generator chip was measured on-wafer in both time and frequency domains using a probe station, digitizing oscilloscope, and spectrum analyzer. To verify the design concept for generating tunable impulse, a separate chip without the pulse-shaping circuitry was first measured. The measured and calculated impulse signals with different durations are shown in Figure 9 for a 50-Ω load condition, and are expectedly similar to the illustrated voltage waveforms at node C shown in Figure 8. Impulse signals having 0.5-1.3 V peak-to-peak voltage with 100-300 ps tunable pulse duration were measured. The pulse duration is defined at 50% of the peak amplitude. The pulse-width tunability is achieved by varying the gate control voltage V_{ctrl} of the tunable delay cell within the range of 0 V to V_{dd} .

Figure 9 also shows clearly that the generated impulse signals have a common falling edge, which is only determined by the falling edge of the square wave at node *B*, while the rising edge of the impulses is affected by the rising edge of the square wave at node *A* and the tunable delay

time. It is noted that the measured waveforms are very symmetrical with almost no distortion. Good symmetry and low distortion are important for most pulse applications. As can be seen, the measured results are well matched to the simulated ones. It should be noted that the final pulse generated consists of three parts: rising edge, tuning delay, and falling edge. For pulses with very narrow width, only the rising and falling edges are involved, resulting in amplitudes much smaller than those for wider pulses. When the pulse width reaches a certain value, the full rising and falling edges and tuning delay all contribute to the pulse generation, so the amplitude does not change anymore and different tuning delays will only change the final pulse width. Consequently, there is not much difference between the amplitudes. Using a better technology such as 0.18-µm CMOS would improve the tuning range of pulses with uniform amplitude.

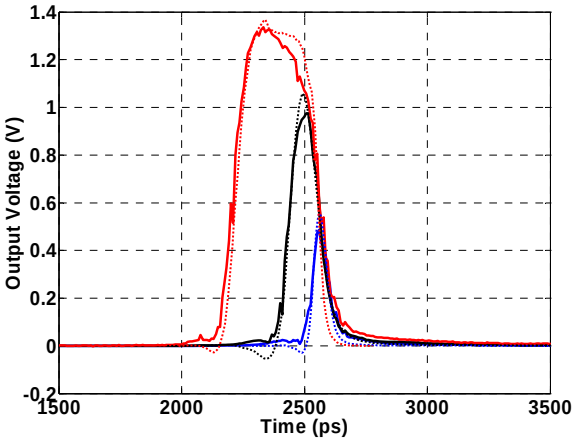


Figure 9 Measured (sold) and calculated (dashed) impulse signals with tunable pulse duration

The measured tunable monocycle pulse signals are shown in Figure 10 for 50 Ω-load condition. By changing the gate control voltage V_{ctrl} of the tunable delay cell in the range of 0 V to V_{dd}, symmetric monocycle pulses with 0.3–0.6 V peak-to-peak voltage and 140–350 ps tunable pulse duration, at 50% of the peak amplitude, were measured, which are also similar to the pulse shapes at node *D* of Figure 8. To verify the frequency response performance of the generated monocycle pulses, the power spectral density (PSD) was also measured using a spectrum analyzer. Figure 11 displays the measured PSD of the monocycle pulse with 140-ps pulse duration, showing that most of PSD is below -50 dBm over the 3.1–10.6 GHz band.

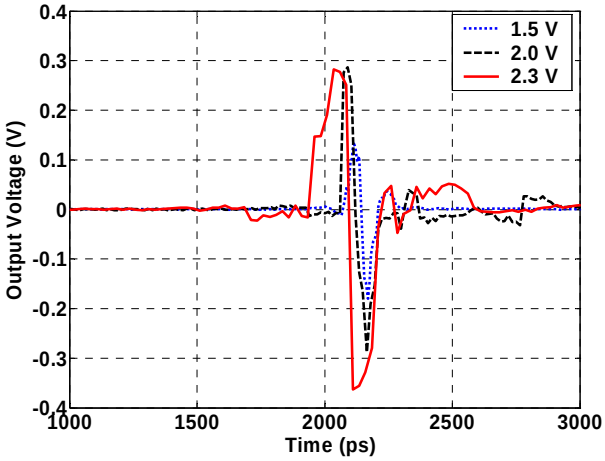


Figure 10 Measured monocycle-pulse signals with tunable pulse duration for different control voltages

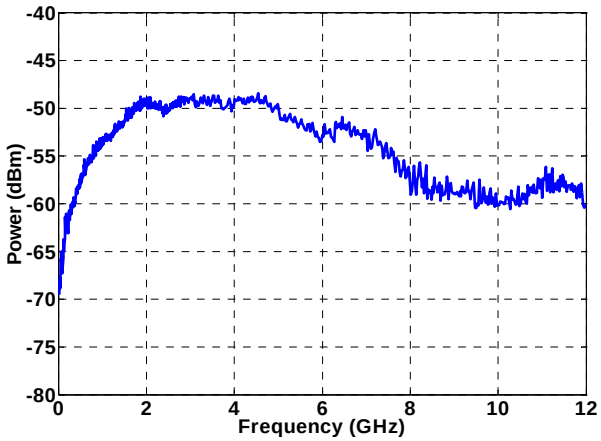


Figure 11 Measured power spectral density of the 140-ps monocycle pulse generated by the pulse generator

4. CONCLUSION

Carrier-based and carrier-less CMOS RFIC UWB transmitters for UWB communication systems, sensors, and radars have been presented. The carrier-based UWB transmitter was implemented using a tunable pulse generator, an UWB SPST switch and an external frequency synthesizer. The transmitter produces UWB signals of different bandwidths ranging from 0.5 to 4 GHz. By varying the LO frequency, the signal spectrum's center frequency can be shifted to any frequency within the UWB band of 3.1-10.6 GHz. The carrier-less UWB transmitter is based on tunable monocycle pulse generator and can generate impulse and monocycle pulse with tunable duration of 100-300 ps and 140-350 ps, respectively. The developed CMOS transmitters are useful for various UWB applications.

5. ACKNOWLEDGEMENT

This work was supported in part by the US National Science Foundation and in part by the US Army - Corps of Engineers.

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