International Journal of Technology (2015) 6: 1050-1056
ISSN 2086-9614 © IJTech 2015

SEEDLESS-ELECTROPLATING PROCESS DEVELOPMENT FOR MICRO-FEATURES REALIZATION

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(Received: June 2014 / Revised: August 2015 / Accepted: October 2015)

ABSTRACT

This study aims to combine the seedless-electroplating process with maskless-lithography, as an alternative for *Lithografie, Galvanoformung, Abformung* (LIGA) or Lithography, Electroplating and Molding with a normal, simpler, and cheaper semiconductor process with tolerable results for nickel electroplating. This study reports the results of various voltages on seedless-electroplating over time, where the optimal combination occurs at an exposure of 7.5 Volts of Direct Current (VDC) for 30 seconds. The thickness of electroplated metal is at a range of ±1.5μm. Moreover, a resolution of ±10μm and roughness (Ra) of ±0.31μm was achieved during the metal deposition process.

Keywords: LIGA; Maskless-lithography; Seedless-electroplating; Wet chemical etching

1. INTRODUCTION

LIGA (*Lithografie, Galvanoformung, Abformung*) is combination of three processes namely lithography, electroplating and molding used in semiconductor technology. LIGA also is commonly used in MEMS (Micro Electro Mechanical System) technology. Therefore, LIGA is a favorable process to realize micro-structures, such as a microfluidics array, an actuator contact pad and interdigitated electrodes (Saile, 2009). The development of this electroplating process was initiated by using synchrotron lithography and a sputtering method to obtain a deposited layer thickness with a range of 25 μm (Becker, et al., 1986). Then, a modification took place to substitute the x-ray source in order to reduce the production cost by using ultraviolet, specifically to have similar quality (Chang & Kim, 2000). Further modifications continued to simplify the LIGA process by using microlens fabrication (Lee, et al., 2002).

This study focuses on developing the seedless-electroplating process at a relatively low cost with simple equipment. Seedless-electroplating is a process that enables the sputtering step to be skipped in metal deposition. Several research groups have initiated and developed seedless-electroplating using different methods (Llona et al., 2006; Zareian-Jahromi & Agah, 2009; Alfeeli et al., 2009; Kumar et al., 2009; Starosvetsky et al., 2010; Lee et al., 2013). The best reported results applied current density between 4 and 5 mA at a bath temperature of 55°C (Llona et al., 2006). Furthermore, in this study we initiated the process to further simplify the procedures by applying visible light lithography combined with seedless-electroplating. This strategy aimed to substitute two conventional steps which are: lithography and metal sputtering with seedless-electroplating and maskless lithography. The first step is done by modifying the light source of the photolithographic process so that it becomes maskless lithography. This step

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Permalink/DOI: http://dx.doi.org/10.14716/ijtech.v6i6.1724

involves an installment of a Digital Light Processing (DLP) projector to replace the need for a photomask. This research has been successfully reported by (Suwandi et al., 2014).

The second part is accomplished by employing seedless-electroplating onto a silicon wafer surface. The silicon wafer surface contains inorganic and organic residues that have a thickness of around 1 nm. Although very thin, this layer can inhibit the flow of electricity from the electrode to the silicon wafer surface. These layers can be removed by a potassium-hydroxide (KOH) etching process. Hence, the seedless-electroplating process can be carried out by eliminating the insulated layer of the silicon wafer. Ultimately, it is expected this new LIGA process will result in a relatively affordable economic outcome.

2. EXPERIMENTAL SETTING

This research was carried out on silicon wafers with a crystal orientation of [1 1 1]. The procedures performed in this experiment include:

2.1. Preparation of Silicon Material

Initially, specimens with a size of 2cm × 3cm were prepared by cutting the silicon wafer. Later, silicone specimens were cleaned with alcohol for 30 seconds and heated at a temperature of $60^{o}C$ to remove possible organic residues.

2.2. Maskless Photolithography

The silicon wafer was coated with a negative – resist from Sigma Aldrich, using spin coating for 30 seconds at 1,000 RPM. The exposure step was conducted for 7 minutes by visible light from a Toshiba TDP - SC25 type DLP projector. The light was set at Red Green Blue (RGB) color module coordinates [0, 176, 240], respectively.

2.3. Electroplating Pretreatment

This process is mainly based on wet chemical etching using a base solution, i.e potassium-hydroxide (KOH). Later, a nitric acid (HNO_3) solution was used to wash specimens for 15 seconds to remove organic residue and further etching, using a hydrofluoric acid (HF) to remove the native oxide for 15 seconds. Finally, an ethanol solution was used to wash specimens for 30 seconds to remove the remaining chemicals.

2.4. Seedless-electroplating

A seedless-electroplating process was carried out by using an electrolyte solution consisting of 300 g of nickel sulfate ($NiSO_4(H_2O)_6$) with 60 g of nickel chloride ($NiCl_2$) and 50 g of boric acid (H_3BO_3). Electrolytes were stirred continuously and maintained at a temperature of around $55^{o}C$ (pH 4 to 4.5) during electroplating. Note that the nickel electrode (anode) was used with a purity level of 95% and specimen as the cathodic part.

2.5. Physical Measurement

Here, we measure several features of the specimen to be used according to the following process parameters:

1. Data on weight change of electroplated silicon wafer by using a Shimadzu Analytical Balance ATY224.
2. Electroplated roughness by measuring the surface of the nickel electroplating using a Surfcom 2900sd3 Accretech.

3. RESULTS AND DISCUSSION

3.1. Seedless-electroplating Characterization

Seedless-electroplating in this research was conducted on silicon wafers [1 1 1] with sizes of 10mm × 10mm. There were two parameters introduced during the process: voltage and

electroplating time. The voltage was set by a commercial adapter. The DC current used in this study are 3, 4.5, 6, 7.5, 9 and 12 volts, respectively. On the other hand, electroplating time is easily adjusted by a chronograph timepiece. The electroplating time was varied at 30, 45, 60, 120 and 240 seconds, respectively. The series of electroplating results can be seen in Figure 1.

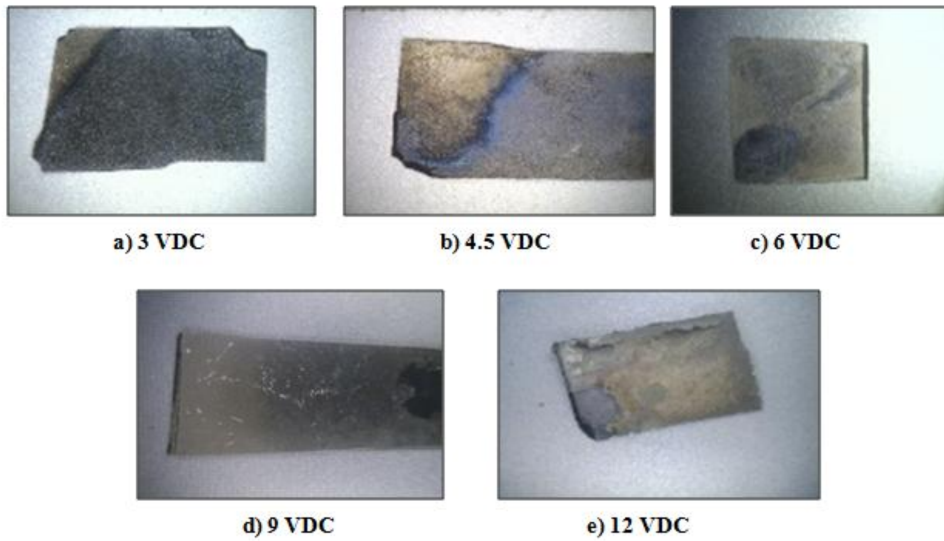


Figure 1 Results of seedless-electroplating based on a combination of plating time and voltage

Figure 1 shows the result of electroplating at 30 seconds using various voltages. It can be seen that at a voltage of 3 and 4.5 VDC, nickel was not deposited over the entire silicon surface. On the other hand, at 6 VDC the nickel deposition almost covers the entire surface of the silicon. At 9 VDC electroplating results in nickel deposition over the entire surface. However, a small delamination on the surface occurred at 12 VDC electroplating with the same exposure time. Ultimately, the electroplated samples were weighed and summarized as shown in Figure 2.

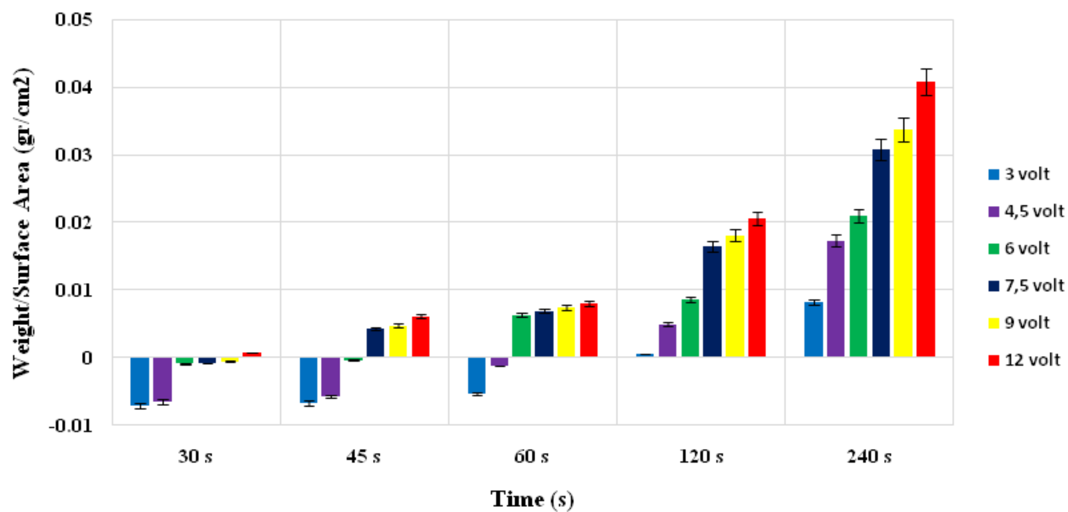
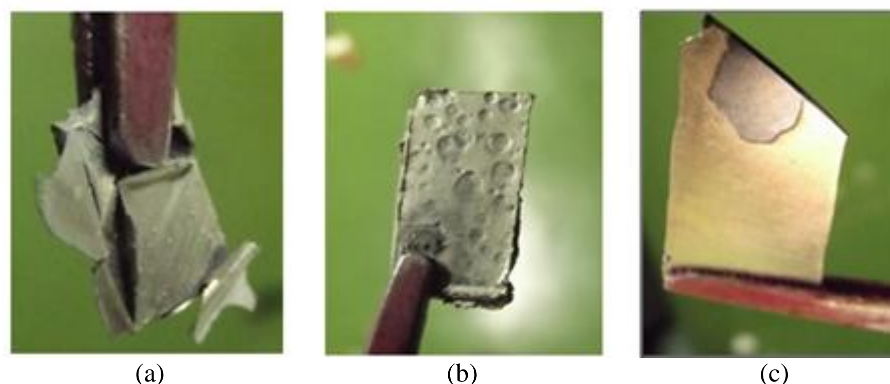


Figure 2 The mass of deposited nickel on the silicon wafer during the electroplating process

Figure 2 indicates the trend of electroplated nickel on the silicon wafer surface. The increasing weight of specimen is assumed to be the nickel from the electroplating. The graph is arranged

based on the two parameters, i.e. voltage (volt) and exposure time (s), in relation to weight/surface area (gm/cm^2). Note that a decreasing weight of the deposition specimen occurs at 30 seconds. It confirms that the chemical substance create pores on the surface during the pretreatment process for electroplating. Later, nickel deposition will be trapped in these pores as a result of the deposition mechanism. Additionally, the delamination phenomenon is directly proportional to voltage and exposure time. The higher the voltage and time, the higher is the evidence of delamination, as depicted in Figure 3a.



(a) (b) (c)

Figure 3 The electroplating process failure by: (a) delamination; (b) trapped air bubbles and; (c) optimum result

Additionally, during the electroplating process, a water-based solution makes the surface of silicon more hydrophobic. This will cause air bubbles to be trapped on the silicon wafer surface. These holes interfere with the plating process on the surface, thus creating an uneven result as shown in Figure 3b. Thereafter, we dipped the silicon wafer into an ethanol solution, prior to the electroplating process. The ethanol will dissolve water and rinse completely the silicon surface from the nickel deposition.

This finding underlined the fact that there are optimum experimental parameters to achieve a good result. Here, the 'good' or desired solution is the full coverage of the specimen without delamination, as shown in Figure 3c. This research also shows that seedless-electroplating indicates an optimal result at 7.5 VDC and 30 seconds exposure time. It also can be concluded that the electroplating process is dependent on voltage and exposure time as explained by Faraday's laws of electrolysis, 1st law and 2nd law. Both of Faraday's laws of electrolysis deduced that the molar mass involved in electrolysis is directly proportional to the electric charge and the element's equivalent weight in an electrolyte solution.

3.2. Surface Roughness

Another measure in material processing is the surface roughness obtained after the process. The roughness (Ra) measure toward deposited nickel is shown in Figure 4 at an average of ± 0.3117µm. The result was acquired using parameters of 7.5 VDC and 30 seconds. Moreover, various voltage results are depicted in Figure 5. The measurements show surface roughness (Ra) average to be in the range of 0.38 to 0.58 µm. These data suggest that nickel plating roughness (Ra) varies at different voltages. However, it appears that the lowest roughness (Ra) value is at 7.5 volts, i.e. 0.31 µm.

Table 1 summarizes the electroplating results in a qualitative manner. A good result was noted by a good coverage of wafer surface (in weight/area) without any delamination and the lowest roughness (Ra) possible. It can be interpreted that a shorter exposure time results in a more favorable outcome. Moreover, a 9 VDC is indicated as the highest current that may be applied

in this process.

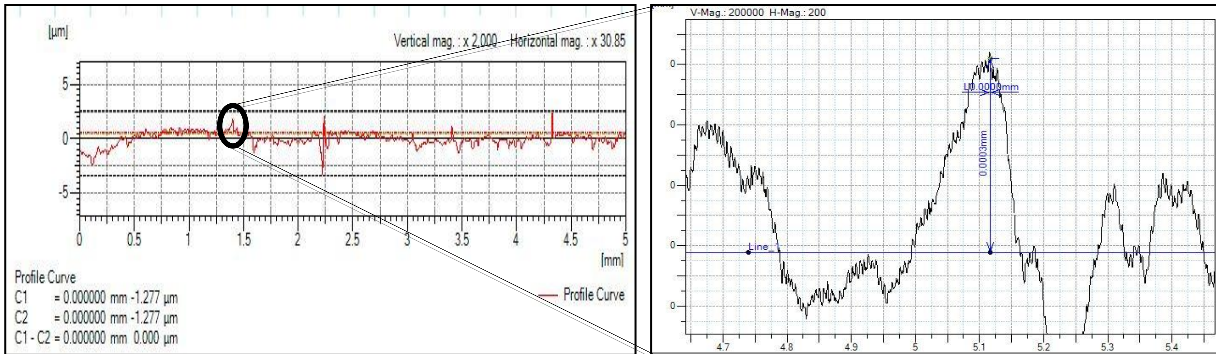


Figure 4 Roughness of electroplated surface at the optimum parameter (7.5 VDC - 30 seconds)

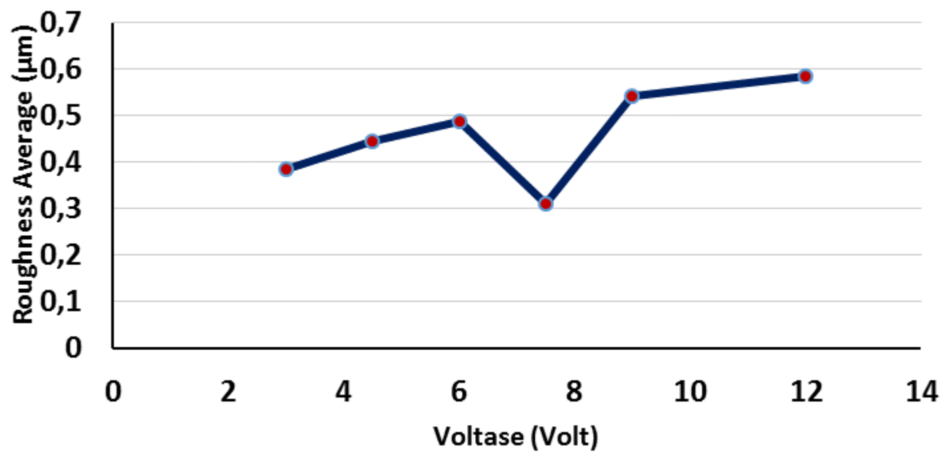


Figure 5 Roughness of electroplated surface at various electroplating voltages

Table 1 Qualitative results of seedless-electroplating (Poor = *, Moderate = **, Good = ***)

Data	3 VDC	4.5 VDC	6 VDC	7.5 VDC	9 VDC	12 VDC
30 s	* * *	* * *	* * *	* * *	* * *	*
45 s	* *	* *	* *	* *	*	*
60 s	* *	*	*	*	*	*
120 s	*	*	*	*	*	*
240 s	*	*	*	*	*	*

3.3. Results of "Budget-LIGA"

Eventually, the lithographic process is simply carried out with a seedless-electroplating method. The lithography realized certain predetermined patterns on the surface of the silicon wafer. A maskless-lithography process that had been studied previously was followed. Later, the electroplating forms a 3D feature on top of the realized pattern within a specific thickness. Ultimately, the realized 3D shall be a mold for a desired structure for a normal LIGA process. Figure 6 shows the result of this "Budget-LIGA" process, thus obtaining a thickness of the deposited nickel in a range of ± 1.5 µm with a resolution of 10µm and a width ranging from ± 2.0 mm.

Later, the seedless-electroplating method was conducted and it obtained a more complex geometry as shown in Figure 7. Smaller dimensions are the objective for the next experiment.

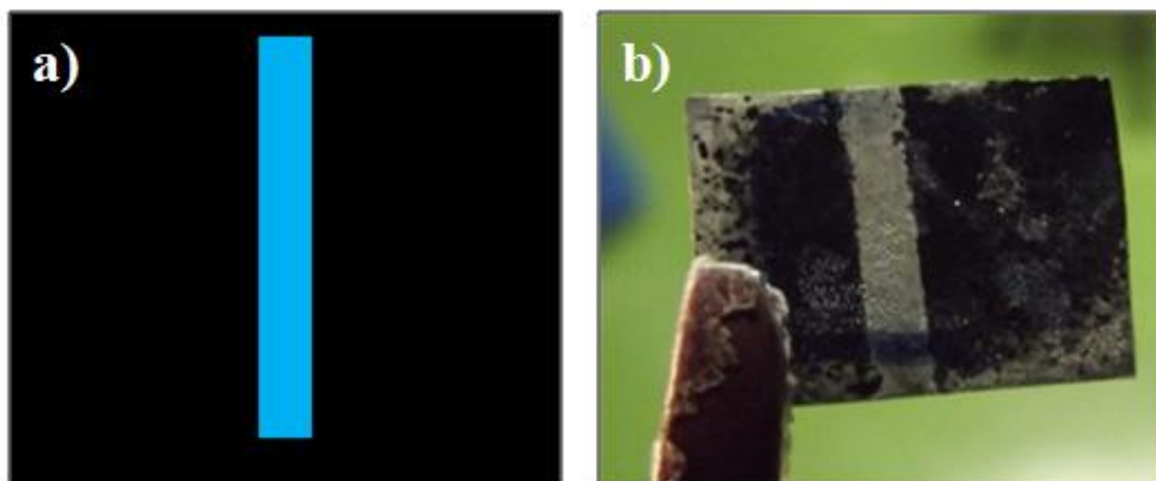


Figure 6 (a) The pattern of maskless-lithography; (b) The result of combined maskless-lithography and seedless-electroplating

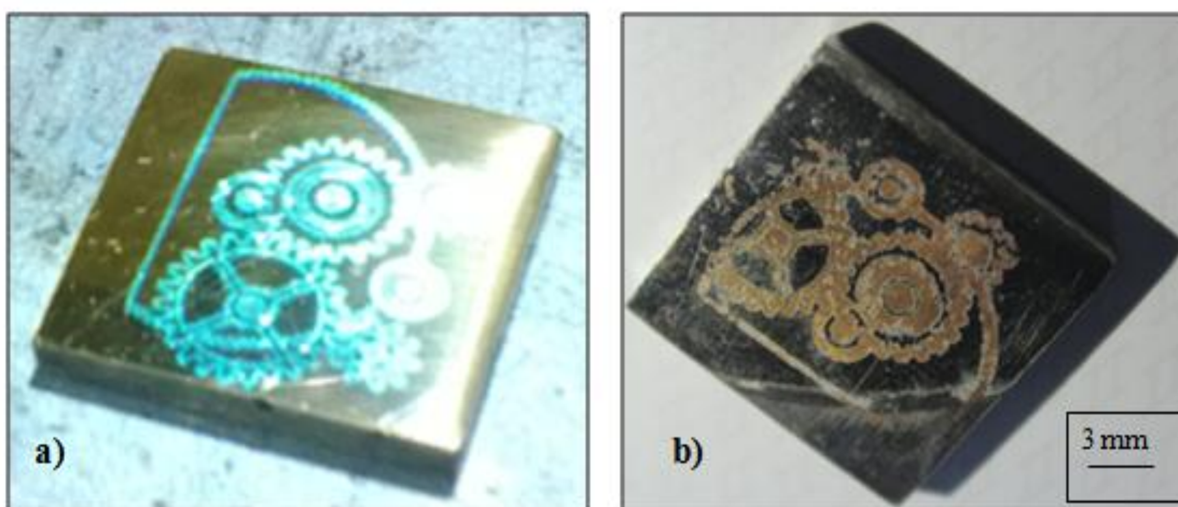


Figure 7 Micro features realization: (a) maskless-lithography process; (b) results of seedless electroplating

4. CONCLUSION

Nickel electroplating without the use of a base layer (sputtering) was successfully carried out to deposit nickel onto a silicon wafer. This was done by eliminating the insulator layer of silicon oxide (SiO_2) on the silicon wafer surface by a wet chemical etching process using potassium-hydroxide (KOH). The optimal parameter for generating a nickel layer on a flat surface without delamination was at a voltage of 7.5 VDC within 30 seconds. The resulting thickness was in the range of 1.5 µm thickness and a roughness (Ra) of 0.3117 µm. The process of "Budget-LIGA" in this study was successfully performed with a combination of maskless-lithography and seedless-electroplating processes.

5. ACKNOWLEDGEMENT

This research was funded by Ministry of Education and Cultural Republic of Indonesia in 2014.

6. REFERENCES

Alfeeli, B., Zareian-Jahromi, M., Agah, M., 2009. Micro Preconcentrator with Seedless Electroplated Gold as Self-heating Adsorbent. In: *Sensors, 2009 IEEE*, pp. 1947−1950

Becker, E., Ehrfeld, W., Hagmann, P., Maner, A., Münchmeyer, D., 1986. Fabrication of Microstructures with High Aspect Ratios and Great Structural Heights by Synchrotron Radiation Lithography, Galvanoforming, and Plastic Moulding (LIGA process). *Microelectronic Engineering*, Volume 4(1), pp. 35−56

Chang, H.K., Kim, Y.K., 2000. UV-LIGA Process for High Aspect Ratio Structure using Stress Barrier and C-shaped Etch Hole. *Sensors and Actuators A: Physical*, Volume 84(3), pp. 342−350

Kumar, S., Greenslit, D., Chakraborty, T., Eisenbraun, E.T., 2009. Atomic Layer Deposition Growth of a Novel Mixed-phase Barrier for Seedless Copper Electroplating Applications. *Journal of Vacuum Science & Technology A*, Volume 27(3), pp. 572−576

Lee, J.Y., Lee, S.W., Lee, S.K., Park, J.H., 2013. Through-glass Copper via using the Glass Reflow and Seedless Electroplating Processes for Wafer-level RF MEMS Packaging. *Journal of Micromechanics and Microengineering*, Volume 23(8), pp. 1−10

Lee, S.K., Lee, K.C., Lee, S.S., 2002. A Simple Method for Microlens Fabrication by the Modified LIGA Process. *Journal of Micromechanics and Microengineering*, Volume 12(3), pp. 334−340

Llona, L.V., Jansen, H.V., Elwenspoek, M.C., 2006. Seedless Electroplating on Patterned Silicon. *Journal of Micromechanics and Microengineering*, Volume 16(6), pp. S1−S6

Saile, V., 2009. Introduction: LIGA and Its Applications, in LIGA and Its Applications (eds V. Saile, U. Wallrabe, O. Tabata and J. G. Korvink), Wiley-VCH Verlag GmbH & Co. KGaA, Weinheim, Germany, pp. 1−10

Starosvetsky, D., Sezin, N., Ein-Eli, Y., 2010. Seedless Copper Electroplating on Ta from a "Single" Electrolytic Bath. *Electrochimica Acta*, Volume 55(5), pp. 1656−1663

Suwandi, D., Whulanza, Y., Istiyanto, J., 2014. Visible Light Maskless Photolithography for Biomachining Application. *Applied Mechanics and Materials*, Volume 493, pp. 552−557

Zareian-Jahromi, M.A., Agah, M., 2009. Self-patterned Seedless Gold Electroplating in High-aspect-ratio Channels for μGC Applications. In: Solid-State Sensors, Actuators and Microsystems Conference, *TRANSDUCERS 2009. International*, pp. 160−163